Final report

1. Project details

Project title	MERGE: Megawatt Scalable Versatile Grid Emulation System
File no.	64020-1065
Name of the funding scheme	Energy Technology Development and Demonstration Program (EUDP)
Project managing company / institution	R&D Test Systems A/S
CVR number (central business register)	37844179
Project partners	AAU-DET (Aalborg University)
Submission date	23 July 2025

2. Summary

Project summary:

The purpose of the project

For grid-code compliance testing of renewable energy resources with ever-increasing power and voltagelevels, a scalable converter-based grid emulator (GE) is an attractive approach. This project focuses on the dynamics analysis, enhanced control and experimental prototype design of the next-generation modular multilevel converter (MMC)-based GE.

Results, conclusions and perspective

Important findings mainly comprise four parts. First, WP2 summarized latest grid codes and testing capability requirements for megawatt GEs. Second, proof-of-concept for hardware and control of the MMC-based GE was conducted through simulation models, identifying dynamics challenges in WP3. Third, WP4 provided specific design guidelines for power hardware, control hardware and enhanced control strategies for the MMC-based GE. Fourth, a controller hardware-in-the-loop (CHIL) testing platform and a megawatt converter-based testbench were developed in WP5 and WP6, respectively. The effectiveness of the proposed control schemes, including the internal submodule (SM) capacitor energy control, the anti-saturation control of transformers and the external voltage/impedance control, was confirmed in the developed setup. The GE successfully reproduced various testing scenarios, e.g., voltage sags, phase jump, impedance variations, harmonics, etc.

In the future, the latest testing capabilities will guide the control and hardware design for practical GEs. The design guidelines of power/control hardware for the MMC-based GE will facilitate the demonstration and transmission of practical projects. The proposed external control and anti-saturation control (ASC) offer feasible solutions to common issues of megawatt GEs worldwide, enhancing their practical significance. The developed CHIL testing platform will be utilized for further research on GEs with higher voltage and power levels.

Projektresumé:

Formålet med projektet

Til Grid-emuleringstest af vedvarende energiressourcer med stigende effekt- og spændingsniveauer er en skalerbar konverterbaseret grid-emulator (GE) en attraktiv tilgang. Dette projekt fokuserer på dynamikanalyse, forbedret kontrol og eksperimentel prototypedesign af næste generations modulære multilevel-konverter (MMC)-baserede Grid-emulatore.

Resultater, konklusioner og perspektiv

De vigtigste resultater omfatter primært fire dele. For det første opsummerede WP2 de seneste grid-koder og testkapacitetskrav for megawatt grid-emulatore. For det andet blev proof-of-concept for hardware og kontrol af den MMC-baserede grid-emulator udført gennem simuleringsmodeller, hvor dynamiske udfordringer blev identificeret i WP3. For det tredje leverede WP4 specifikke designretningslinjer for strømhardware, kontrolhardware og forbedrede kontrolstrategier for den MMC-baserede GE. For det fjerde blev der udviklet en controller hardware-in-the-loop (CHIL) testplatform og en megawatt-konverterbaseret testbænk i henholdsvis WP5 og WP6. Effektiviteten af de foreslåede kontrolanordninger, herunder den interne submodule-kondensatorstyring, anti-saturation kontrol af transformatorer og den eksterne spændings-/impedansstyring, blev bekræftet i det udviklede setup. Grid-emulatoren reproducerede med succes forskellige testscenarier, såsom spændingssving, fasehop, impedansvariationer, harmoniske udsving, osv.

I fremtiden vil de nyeste testmuligheder vejlede kontrol- og hardware-designet for praktiske grid-emulatorer. Designretningslinjerne for strøm-/kontrolhardware til MMC-baserede grid-emulatorer vil lette demonstrationen og transmissionen af praktiske projekter. De foreslåede eksterne kontrol- og anti-saturation kontroltiltag tilbyder realistiske løsninger på almindelige problemer med megawatt grid-emulatorer over hele verden og forbedrer deres praktiske betydning. Den udviklede CHIL-testplatform vil blive anvendt til yderligere forskning i grid-emulatorer med højere spændings- og effektniveauer.

3. Project objectives

This project aims to analyse the dynamics challenges, propose enhanced control schemes and develop a prototype for the MMC-based GE, which is used for grid-code compliance test of renewable energy resources according to the latest grid codes and standards. Sub-objectives are outlined below:

- Identify the latest testing capability requirements for GEs following the state-of-the-art grid codes and standards.
- Design the power hardware of the MMC-based GE, specifically for the number of SMs per arm, arm inductance, SM capacitance and step-up transformers.
- Perform concept analysis of the MMC-based GE alongside proof-of-concept simulation models on how the testing capabilities should be achieved.

- Figure out the dynamics challenges and propose the enhanced control schemes of the MMC-based GE when implementing various testing capabilities.
- Develop the CHIL and megawatt converter-based prototype to validate the effectiveness of the proposed control approaches.

4. Project implementation

The project started out with a highly motivated team, and the first three work packages went according to the plan, with extensive research an analysis of the market and requirements and a promising theoretical framework. Then the project started to focus more on the hardware part of it, and to investigate different designs and ways to manufacture the 1 MW demonstrator that was originally planned to produce within the project. As it turned out the price for such a demonstrator was more expensive than anticipated, which by far exceeded the budget for the project. Different options related to seeking commitment from potential customers to reduce the risk of ending up purchasing expensive equipment that could not be sold, was considered, but it was not possible to get this commitment at this early-stage development and lack of track record.

Based on not being able to purchase the original planned hardware setup, alternative solutions for reaching the goals of the project with less expensive hardware was evaluated. This resulted in a change of the prototype 1 setup, from a small-scale demonstrator to an even smaller scale CHIL setup, but with the ability to still run almost all the simulations and tests originally planned.

After the concept of the setup was fixed, the project evolved into a design phase, both the CHIL hardware design and the control software. The CHIL setup ended up being a huge success, and being the main driver of the project with numerous tests being executed and the setup was continuously upgraded and improved throughout the project.

Going into the second half of the project a few resignations and change of personal connected to the project slowed down the process in the project significantly. At the same time, it turned out to be much harder than anticipated to finalize the deal with an OEM to be able to use their equipment for a full-scale test/demonstration (Prototype 2). Those two things together resulted in a need to extend the timeline of the project with a year.

The final stage of the project depended a lot on finding a partner that would allow the project to use their equipment for a full-scale test. This didn’t happen until the very end of the project, and with another grid emulation concept than what the project had been focusing on. It was still possible to test a lot of the control algorithms developed in the project, some of them with a bit of modification. The full-scale testing was done to a smaller extend than planned but was still able to verify the simulations done in the project.

5. Project results

The objective of the project has been changed a bit from the original. It was planned to manufacture a 1 MVA MMC-based Grid emulator, but due to circumstances described in chapter 4, it was replaced by the CHIL testing platform and a 2-level megawatt converter-based testbench.

Some of the key accomplishments from the project are listed as the following 5 parts. For more technical details of the findings and results, please lookup the corresponding publications as referred to. A list of publications is found in chapter 8. Appendices.

5.1 Power-hardware design and topologies of converter-based grid emulators [J1]

This work identifies first the power rating of future GEs based on the system architecture and the evolution of device under tests (DUTs). The converter topologies of GEs are then evaluated to identify the potential GEs for high scalability. Design considerations of power semiconductor devices, step-up transformers, dc choppers and dc capacitors are also discussed for existing and prospective GEs.

1) System architecture and power rating

Fig. 1 shows a general structure of a converter-based GE system. Recently, the converter-based GEs have become increasingly prominent in testing grid-code compliance of renewable energy resources and energy storage systems, i.e., DUTs. The GE typically uses a back-to-back (BTB) structure, comprising the active-front-end (AFE) converter and the controlled voltage generator (CVG) [J1]. In the testing system, the power and voltage ratings of the DUTs are steadily increasing. Fig. 2 summarizes the power ratings of typical type-III and type-IV wind turbines (WTs). Currently, individual type-III and type-IV WTs can reach power capacities of up to 7 MW and 16 MW, respectively. Future developments anticipate WTs with capacities of 18 MW and even 20 MW from companies like GOLDWIND and MINGYANG SMART ENERGY [J1]. Additionally, to avoid using cables with excessively large diameters, the voltage level in wind power plant transmission systems has been raised from 11 kV to 66 kV, with potential increases to 132 kV [J1].

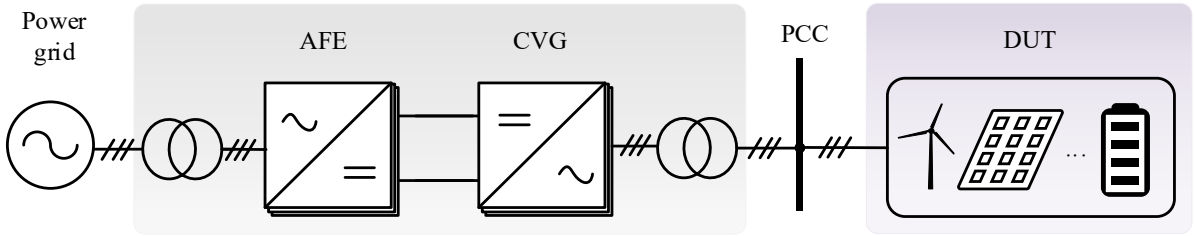


Fig. 1 General structure of a converter-based GE system [J2].

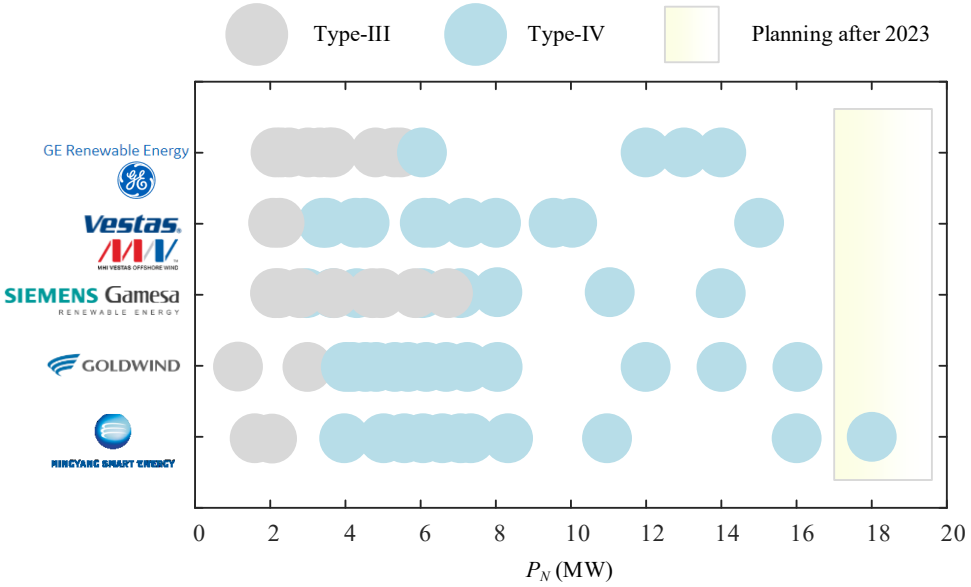


Fig. 2 Power ratings of type-III and type-IV WTs [J1].

To perform the grid-code compliance test of these WTs, the continuous power rating and PCC voltage of the converter-based GE should be at least 20 MW and 66 kV or even 132 kV, respectively. Moreover, the type-IV WTs typically have a maximum short-circuit current capacity of 2 p.u., while the type-III WTs can handle an overcurrent up to 7 p.u. During fault ride-through (FRT) tests, the GE must cover a broad range of under- and overvoltage, i.e., 0%-160% of rated voltage [J2]. The worst scenario assumes that the WT delivers the maximum current to ride through the 160% of rated voltage. According to Fig. 2 and [J1], the maximum power responses of type-IV and type-III WTs are 64 MVA and 78.4 MVA. Thus, the short-term power capacity of a future GE should be at least 80 MVA.

2) Topology comparison

Fig. 3 illustrates the scalable topologies of converter-based GEs. To accommodate the growing power and voltage ratings of DUTs, a scalable GE system is required. The interleaved neutral point clamped (NPC) converters that are interfaced with a multi-winding transformer are commonly founded in GE systems. While

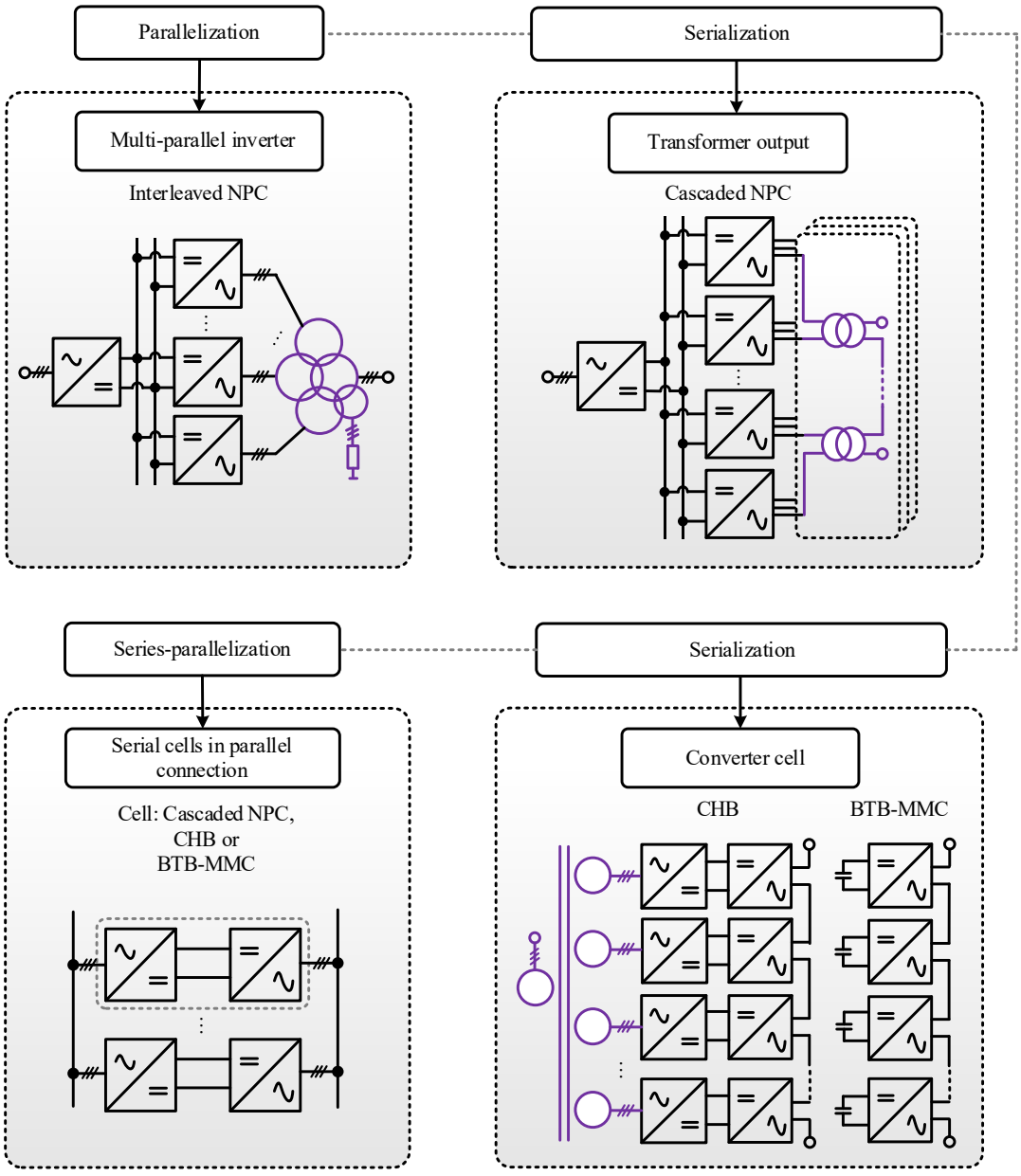


Fig. 3 Scalable topologies of typical converter-based GEs [J1].

increasing the number of NPC converters yields a higher power rating, the circulating current among interleaved converters and manufacturing process of multi-winding transformers may limit the system scalability. Instead of using a multi-winding transformer, multiple single-phase transformers with a customized configuration are used to eliminate the circulating current among the NPC converters. In this configuration, the secondary windings of single-phase transformers are connected in series, summing up the terminal voltages of NPC converters, thus called the cascaded NPC-based GE. Yet, as the number of NPC converters increases, different parasitic parameters among these single-phase transformers may distort the emulated voltage at the point of common coupling (PCC).

Alternatively, a two-winding step-up transformer along with multilevel converters, e.g., the cascaded H-bridge (CHB) converter and the MMC can be also used with GEs. In the CHB-based GE, the dc link of each H-bridge cell converter is supplied by a three-phase AFE converter. All AFE converters are connected to the grid via input multi-winding transformers. The number of windings and the manufacturing procedure of multi-winding transformers restrict the scalability of a CHB-based GE. In contrast, the MMC-based GE has a common dc link, allowing it to use numerous SMs per arm and two-winding transformers to realize the desired voltage and power ratings.

Table I shows specific comparison of four typical converter-based GEs. Several perspectives are discussed, such as the number of output voltage levels, the PCC voltage distortion, the use of ac filters, the complexity of manufacturing transformers, and the voltage and current stresses on power semiconductor devices, etc. It is found that the MMC-based GE has been identified as a promising approach for future medium to high-voltage grid emulation, such as in the 66 kV to 132 kV range. Consequently, this project focuses on the development of an MMC-based GE.

Table I Specific comparison of four typical GEs [J1]

Typical GEs	Interleaved NPC	Cascaded NPC	CHB	BTB-MMC
Number of output line-to-neutral voltage levels	$2N_{npc}+1$	$2N_{npc}+1$ (N_{npc} is even)	$2N_H+1$	$2N_{HB}+1$ for HBSM-based $4N_{FB}+1$ for FBSM-based
CVG-side ac filter	Integrated with CVG-side TR (*RC* filter)	Connected to the PCC (*RC* filter)	Connected to ac terminal of CVG (*LC*/*RLC* filter) or filterless	Connected to ac terminal of CVG (*C*/*RC* filter) or filterless
AFE-side transformer (TR)	Standard or multi-winding	Standard or multi-winding	Single multi-winding or Several multi-winding	Standard
CVG-side TR	Multi-winding	Single-phase and custom-built	Standard	Standard
Scalability	Low	Moderate	Moderate	High
Number of semiconductor devices in the AFE	≥3×6	≥3×6	$3\times6N_H$	$6\times2N_{HB}$ for HBSM-based $6\times4N_{FB}$ for FBSM-based
Number of semiconductor devices in the CVG	$3\times6N_{npc}$	$3\times6N_{npc}$	$3\times4N_H$	$6\times2N_{HB}$ for HBSM-based $6\times4N_{FB}$ for FBSM-based
Voltage stress of semiconductor devices in the CVG	$0.5V_{dc}$	$0.5V_{dc}$	V_{cell}	V_{sm}
Current stress of semiconductor devices in the CVG	$I_{pcc}N_{tr}/N_{npc}+$ $(1\text{-}1/N_{npc})N_{tr}V_{dc}/(2Z_{in})$	$I_{pcc}N_{tr}$	$I_{pcc}N_{tr}$	$I_{cir}+I_{pcc}N_{tr}/2$
Advantages	▪ High technology readiness level of interleaved NPCs	▪ Low step-up ratio of custom-built TRs ▪ No circulating current between NPC inverters	▪ No circulating current between H-bridge cells ▪ Filterless is feasible	▪ Using standard transformers ▪ Filterless is feasible
Disadvantages	▪ Circulating current between NPCs related to Z_{in} ▪ Manufacturing complexity of multi-winding TRs	▪ Bulky volume of ac filter as the V_{pcc} increases ▪ Manufacturing complexity of custom-built TRs	▪ Manufacturing complexity of multi-winding TRs	▪ Fluctuations of SM capacitor voltage and circulating current ▪ Bulky SM capacitors and arm inductors

3) Design considerations

Fig. 4 illustrates the design challenges of power components in the typical converter-based GEs, including power semiconductor devices, CVG-side transformer, dc-link chopper, neutral-point (NP)/cell/SM capacitors and switchgear. To address these challenges, design considerations of power components in GEs have also been presented, such as the oversized design of power semiconductor devices, the choice of dc-link choppers, the anti-saturation design of transformers, and the double insulation of switchgear. For further details, please see [J1].

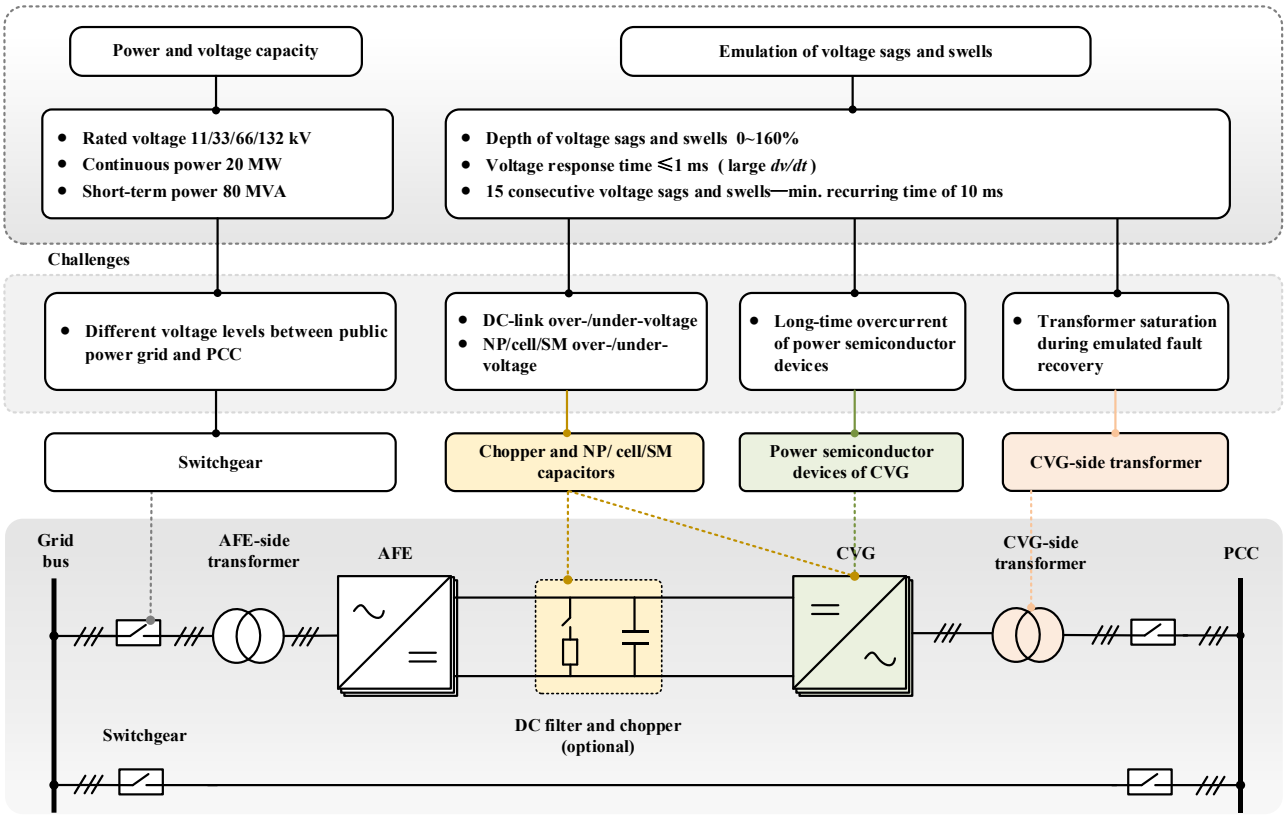


Fig. 4 Design challenges of power hardware in converter-based GEs [J1].

5.2 Overview of testing capabilities and dynamics challenges [J2] [C1]

This work first reviews testing capability requirements for GEs based on the latest grid codes and standards. Then, dynamic interactions and control solutions in typical converter-based GEs are discussed when implementing the testing capabilities.

1) Latest grid codes and testing capabilities for GEs

Fig. 5 summarizes the latest updates of grid codes, standards and testing capability requirements of GEs. The testing capabilities are discussed across five dimensions: emulating voltage sags and swells, synthesizing grid impedance, generating flickers and harmonic voltage, reproducing grid frequency deviation, and the provision of these testing capabilities simultaneously. For more specific grid codes, standards and testing capability requirements, please see the cited papers in [J2].

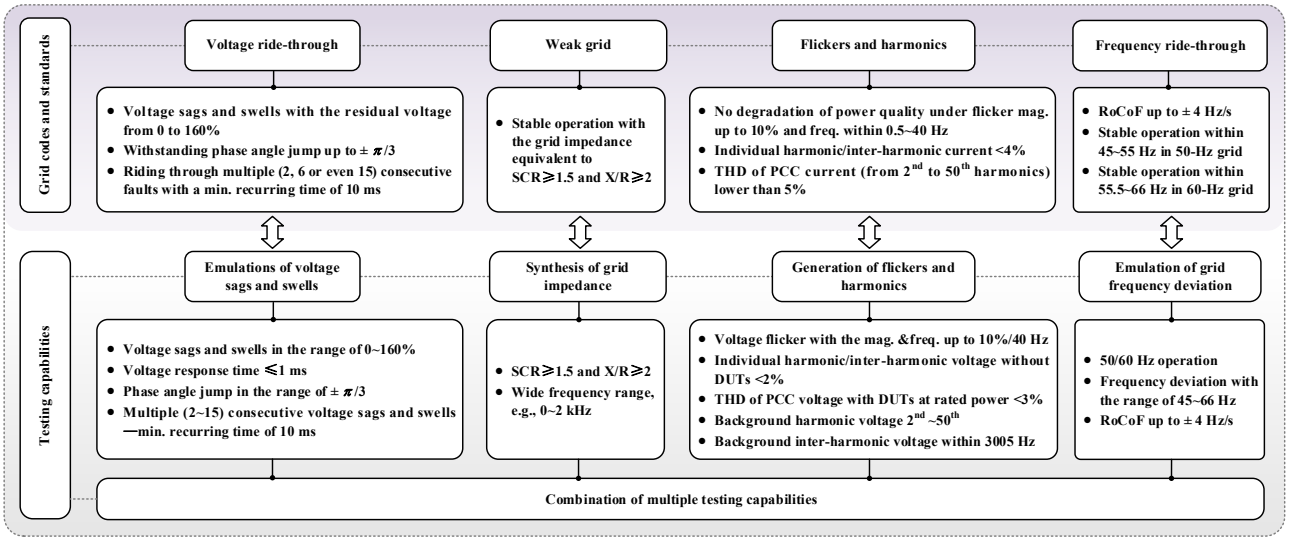


Fig. 5 Latest updates of grid codes and testing capability requirements of GEs [J2].

2) Dynamic challenges

When reproducing voltage sags/swells, phase jumps and grid impedance variations in grid faults, the DUT may inject significant fault current into the GE as per the FRT request. In such scenarios, MMC-based GEs may experience several issues with its SM capacitors and the step-up transformer, and may even interact with the DUT, causing instability issues. Fig. 6 shows typical dynamics challenges in the MMC-based GE.

- Transient overvoltage and voltage imbalances in SM capacitors: In FRT tests, DUTs may inject both current overshoot at the fault inception and a sustained during-fault overcurrent into the MMC-based GE. For instance, type-IV WTs can inject a transient fault current of 2 p.u. and a continuous overcurrent up to 1.5 p.u. Changes in the PCC voltage and the fault current tend to induce different charging currents for the upper-arm and lower-arm SM capacitors, which lead to transient overvoltage and continuous voltage imbalances in SM capacitors, particularly when the residual PCC voltage approaches zero. In turn, the

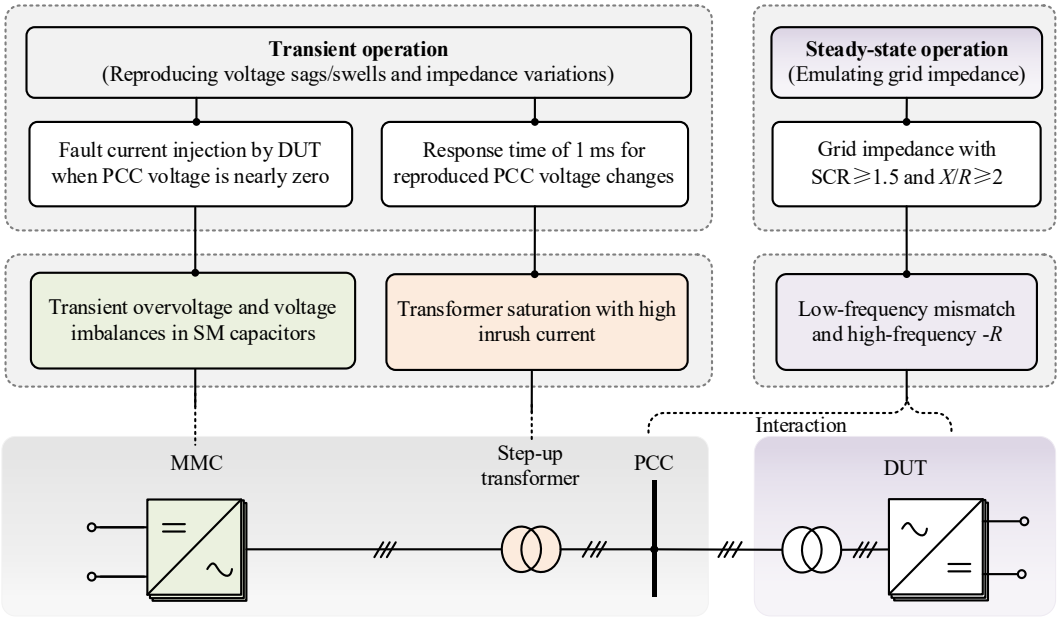


Fig. 6 Typical dynamics challenges in the MMC-based GE [J2].

SM capacitor voltage overshoot and imbalances may introduce undesired harmonics into the emulated PCC voltage or even lead to trips and malfunctions of the GE. In the normal operation of the GE, the adverse effects of SM capacitor dynamics on the output voltage of MMC can be addressed by a closed-loop modulation scheme with the SM capacitor energy balancing control (EBC). However, as found in this project, the traditional EBC scheme fails to mitigate the transient overvoltage and voltage imbalances issues when the MMC-based GE reproduces nearly zero grid voltage.

- Step-up transformer saturation: DNV imposes a stringent requirement on the response time of GEs for emulating a voltage sag/ swell, which should be within 1 ms. This sudden change in the PCC voltage may induce a notable dc offset of magnetic flux in the GE output transformer, potentially leading to a dc magnetic current surge. This inrush current may be 2~10 times of the rated current of transformer, which not only distorts the emulated PCC voltage, but may even activate the overcurrent protection of the MMC-based GE, tripping the overall system.

- Low-frequency inaccurate impedance emulation and high-frequency negative resistance: Grid faults typically give rise to simultaneous changes with voltage magnitude and grid impedance at the PCC. In the post-fault process, a high-impedance grid can lead to transient overvoltage at the PCC or even low-frequency (<100 Hz) oscillations. Consequently, the metrics of grid strength are continuously updated for testing the grid-code compliance of DUTs. For instance, Australian Energy Market Operator (AEMO) requires DUTs to maintain stable operation with a minimum SCR of 1.5 and a X/R ratio of at least 2. Therefore, it is important for a GE to accurately synthesize the steady-state and transiently varying grid impedance, thereby reproducing the overvoltage and voltage oscillations. Yet, the time delay and control plant of a converter-based GE may affect the accuracy of impedance emulation, particularly in the low-frequency range. Further, the time delay tends to introduce a negative resistance (-*R*) into the emulated impedance of the GE in the high-frequency range. This -*R* may cause unexpected harmonic instability issues.

The dynamics analysis and enhanced control schemes for the MMC-based GE are then discussed in this project to address three identified dynamics challenges.

5.3 Mitigation of overvoltage and voltage imbalances in SM capacitors [J3] [C2]

This work identifies the root causes of transient overvoltage and voltage imbalances in SM capacitors, an averaged model of the MMC-based GE is developed. It is revealed that both the emulated voltage changes and the fault current injected by a DUT contributed to the issues, which cannot be addressed by the classical internal control of the MMC. Afterwards, an enhanced SM capacitor EBC approach is proposed. This method effectively mitigates both transient overvoltage and voltage imbalances, ensuring that the SM capacitor voltages are within 70%~110% of the nominal value, even when the emulated PCC voltage is nearly zero.

1) System description

Fig. 7 depicts the topology of the MMC-based GE. *N* full-bridge submodules (FBSMs) in series connection are used in each arm of the MMC. Negative voltages can be generated by these FBSMs at their ac sides, which realizes the modulation index of the MMC higher than 1, thereby improving the utilization ratio of the dc-link voltage. L_{arm}, R_{arm}, C_{sm} and V_c denote the arm inductance, arm resistance, SM capacitance and rated SM capacitor voltage, respectively. V_{dc} (i_{dc}), v_{1j} (i_{1j}) and v_{pccj} (i_{pccj}) are the dc-link, primary-side and PCC-side voltages (currents), respectively. *j* denotes phase *a*, *b* or *c*. N_{tr} is the turn ratio of the GE transformer.

Fig. 8 shows the single-line model of the MMC-based GE. i_{uj} (v_{uj}) and i_{lj} (v_{lj}) are the upper- and lower-arm currents (voltages), respectively. i_{cirj} is the circulating current. n_{uj} and n_{lj} are the insertion indices for the upper-

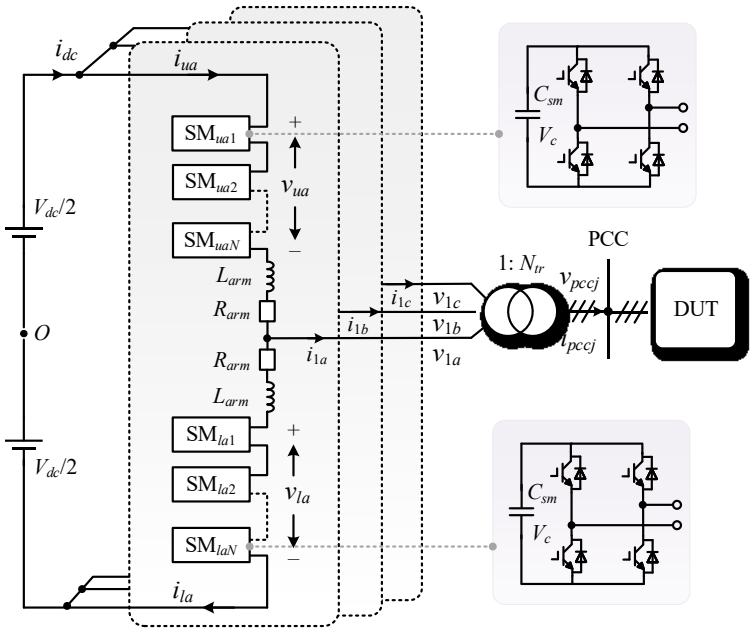


Fig. 7 Topology of the MMC-based GE [J3] [C2].

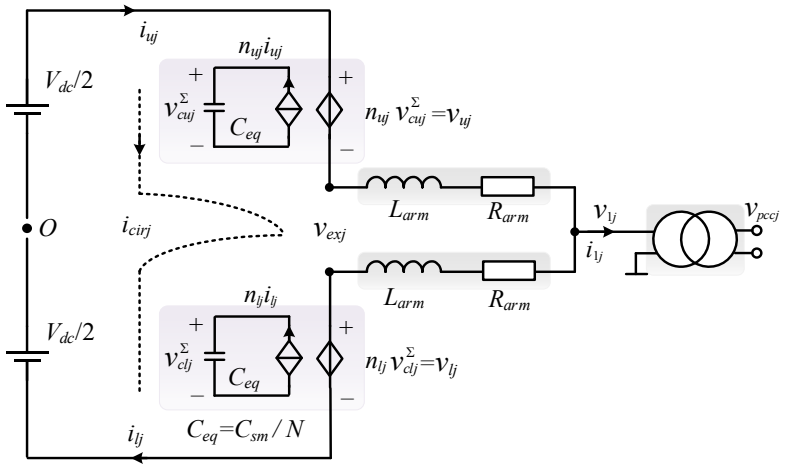
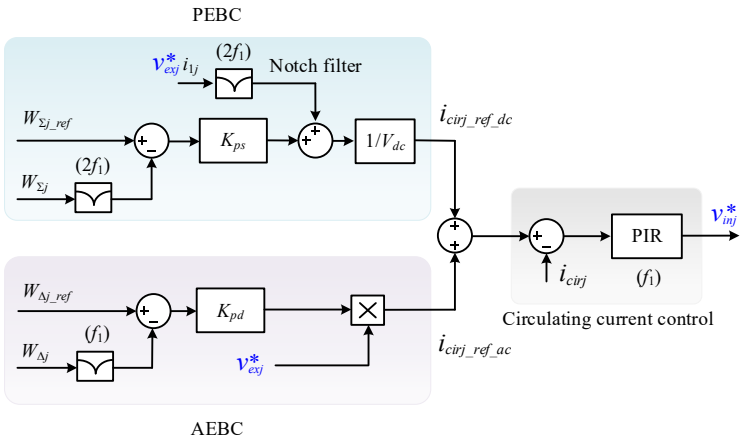


Fig. 8 Single-line model of an MMC-based GE [J3] [C2].



(a)

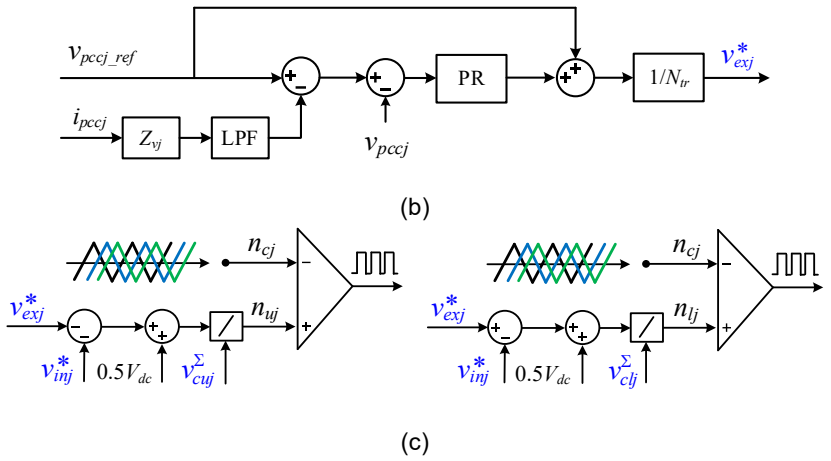


Fig. 9 Typical control and modulation diagrams of the MMC-based GE. (a) Traditional internal EBC. (b) External control. (c) Closed-loop PSC-PWM [J3].

and lower-arm SMs. To realize the desired output voltage, the internal control and the external control are needed in the MMC to regulate v_{inj} and v_{exj}, respectively [J3].

Fig. 9 depicts the general control and modulation diagrams of the MMC-based GE. Fig. 9(a) shows the traditional internal control. The phase energy balancing control (PEBC) is employed to generate a dc circulating current $i_{cirj\_ref\_dc}$ for controlling the energy sum of each-phase SM capacitors to track its reference $W_{\Sigma j\_ref}$. The arm energy balancing control (AEBC) aims at injecting a fundamental-frequency circulating current $i_{cirj\_ref\_ac}$ for balancing the upper- and lower-arm SM capacitor voltages. The inner circulating current control generally utilizes the proportional-integral-resonant (PIR) controller to adjust i_{cirj} for precisely tracking $i_{cirj\_ref\_dc}$ and $i_{cirj\_ref\_ac}$.

Fig. 9(b) shows a typical external control diagram, which comprises the proportional-resonant (PR) controller-based voltage control (VC) and the virtual impedance (VI) control. They are employed to reproduce the dynamics of grid faults, i.e., the voltage sags with grid impedance variations, through adjusting the external control output command v^*_{exj}. The database of the emulated grid faults, e.g., the fault depth D, the fault inception t_{sag}, the fault clearing instant t_{rec}, the pre-fault grid impedance Z_g and the during-fault equivalent grid impedance Z_{eqf} are configured in the PCC voltage reference v_{pccj_ref} and the emulated impedance Z_{vj}. For more details of v_{pccj_ref} and Z_{vj}, please see [J3].

Fig. 9(c) shows the closed-loop phase-shifted-carrier (PSC) pulse width modulation (PWM) scheme, which is used to alleviate the adverse impact of internal SM capacitor voltages (v_{cuj} and v_{clj}) on the ac-side output dynamics (v_{exj}) of MMC.

2) Problem statement

Taking the emulation of three-phase balanced fault as an example, Fig. 10 shows the adverse influence of i_{pccj} on the SM capacitor dynamics of the MMC-based GE. According to [J3], Fig. 8 and Fig. 10, the mechanism of transient overvoltage and voltage imbalances during grid faults is discussed as follows.

- Transient overvoltage: i_{pccj} generally consists of a transient current overshoot i_{pcc_tr} and a continuous overcurrent i_{pcc_co} during grid faults. For v_{cuj} and v_{clj}, the dc components v_{cuj_dc} and v_{clj_dc} are mainly dependent on i_{pcc_tr}, while the ac components v_{cuj_ac} and v_{clj_ac} depend on i_{pcc_co} [J3]. Both dc and ac components around t_{sag} determine the transient SM capacitor overvoltage.

- Voltage imbalances: i_{pccj} has an inverse impact on the charging currents of the upper- and lower-arm SM capacitors, leading to opposite signs between v_{cuj_dc} and v_{clj_dc} [J3]. The changes with v_{cuj_dc} and v_{clj_dc},

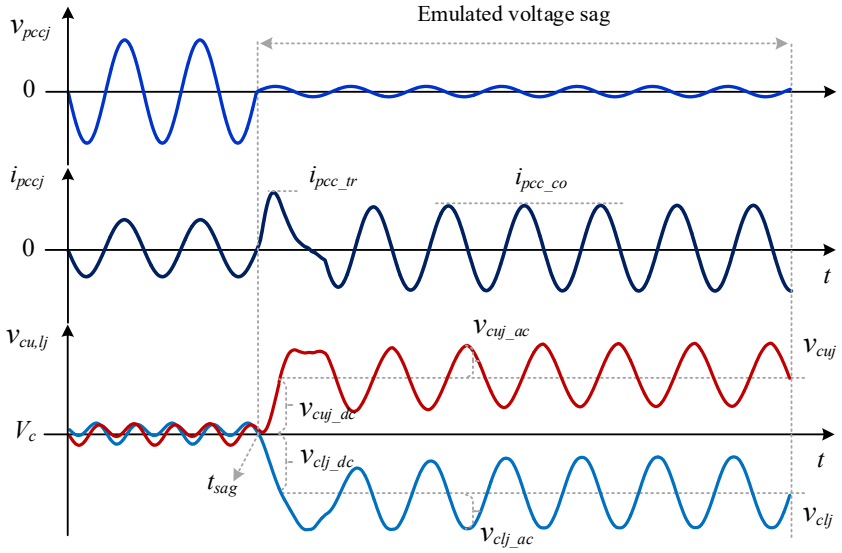


Fig. 10 Impact of current injection by a DUT on SM capacitor voltages [J3].

proportional to the transient current overshoot i_{pcc_tr}, contribute to the voltage imbalances in the upper- and lower-arm SM capacitors.

3) Enhanced control method

Fig. 11 shows the diagram of the enhanced SM capacitor EBC scheme. Firstly, incorporating reference scaling factor k_n into the PEBC is used to mitigate transient SM capacitor overvoltage. $k_n \leq 1$ is activated for each fault-emulation phase j, whereas it is deactivated for the normal operation and the non-fault phase. Further, the activation of k_n is dependent on the setting of v_{pccj_ref}, i.e., D, t_{sag} and t_{rec}. Specific design guideline for k_n are provided in [J3] considering the constraints of upper/lower voltage limits, overmodulation and SM capacitor voltage ripple.

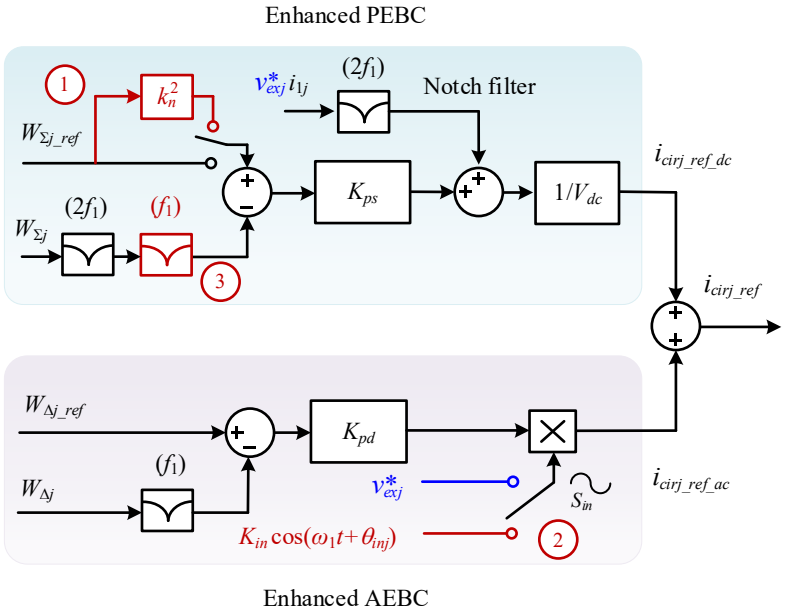


Fig. 11 Diagram of the enhanced SM capacitor EBC [J3].

Secondly, injecting a specific fundamental-frequency circulating current by the AEBC is adopted to alleviate the SM capacitor voltage imbalances. S_{in} denotes the total injected sinusoidal signal. For the fault-emulation phase j, the injected signal $K_{in}\cos(\omega_1 t+\theta_{inj})$ is activated, where K_{in}, ω_1 and θ_{inj} denote its magnitude, angular fundamental frequency and phase angle, respectively. In this case, the magnitude of i_{cirj_ac} is proportional to K_{in} instead of v^*_{exj}. For the normal operation and non-fault phase, v^*_{exj} contributes to S_{in}. For further detailed design guidelines for K_{in} and θ_{inj}, please see [J3].

Thirdly, as found in [J3], the PEBC also generates an undesired fundamental-frequency signal during grid fault emulation, which reduces the efficacy of the AEBC. To address this issue, an extra notch filter tuned at the fundamental frequency (f_1) is incorporated into the PEBC.

4) CHIL validation

Fig. 12 illustrates the CHIL testing setup for the MMC-based GE and a grid-following (GFL) DUT based on the MicroLabBox and RT Box 3. The MicroLabBox is used as the control hardware for the MMC, executing the discretized control and the database of v_{pccj_ref} and Z_{vj}. The RT Box 3 utilizes three cores for the real-time simulation. The main circuits of MMC featuring 4 FBSMs per arm with transformers and a DUT are simulated in Core 1. Core 2 implements a general GFL control for the DUT. Core 3 specifies the I/Os of the RT Box used to interface with the MicroLabBox.

Fig. 13 depicts a general GFL control of the DUT based on a type-IV WT inverter. For simplicity, the averaged model of the WT inverter is used. The second-order generalized integrator phase-locked loop (SOGI-PLL) is utilized to track the positive-sequence phase angle of the reproduced grid. Following the grid-code require

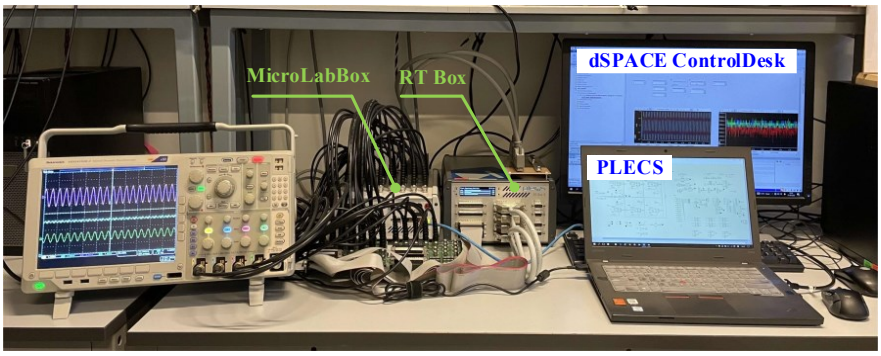


Fig. 12 CHIL test setup [J3].

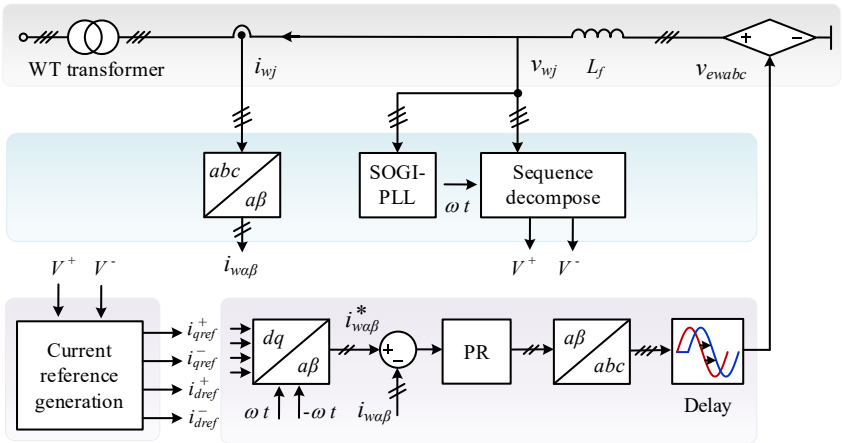
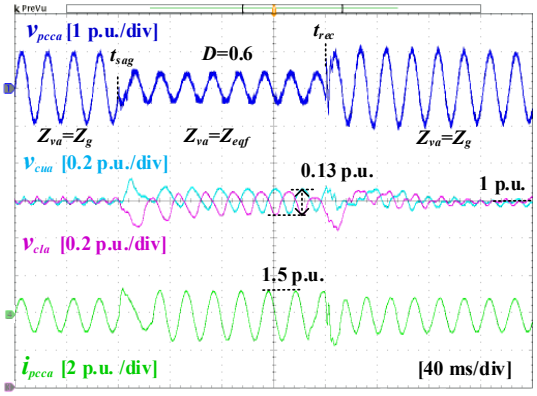


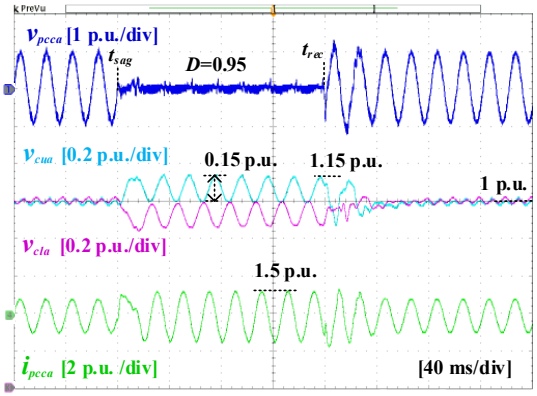
Fig. 13 An example for the GFL control of DUT [J3].

ments, the positive- and negative-sequence current references can be acquired in the *dq* frame. After the *dq*/$\alpha\beta$ transformation, the GFL control in the $\alpha\beta$ frame can be implemented for the DUT. To analyze the influence of different transient fault currents injected by the DUT on SM capacitor voltages, regulating the controller parameters of the GFL control is a straightforward solution.

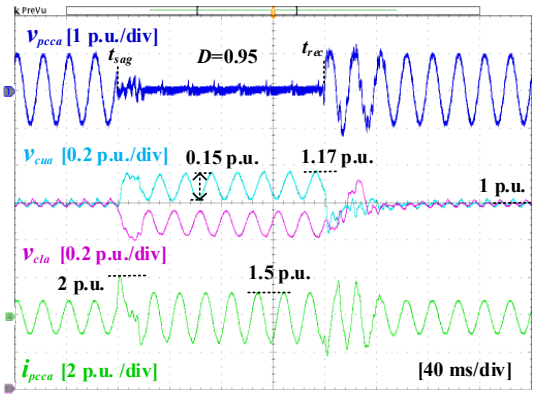
Fig. 14 illustrates the CHIL results for an MMC-based GE using the traditional EBC during a balanced fault emulation. In the oscilloscope, Channel 1 (v_{pcca}) and Channel 4 (i_{pcca}) are the phase-*a* voltage and current at



(a)



(b)



(c)

Fig. 14 FRT testing results by an MMC-based GE based on the traditional EBC. (a) I_{pcc_max}=1.5 p.u. and *D*=0.6. (b) I_{pcc_max}=1.5 p.u. and *D*=0.95. (c) I_{pcc_max}=2 p.u. and *D*=0.95 [J3].

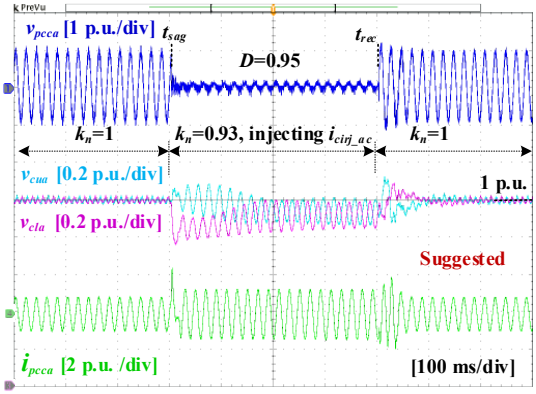


Fig. 15 FRT testing results by an MMC-based GE based on the enhanced EBC.

the PCC. Channel 2 (v_{cua}) and Channel 3 (v_{cla}) denote the averaged voltage of upper- and lower-arm SM capacitors in phase *a*, respectively. During normal operation, the dc voltage of v_{cua} and v_{cla} is the rated voltage i.e., 1 p.u., of SM capacitors.

In Fig. 14(a), a voltage sag with residual PCC voltage of 0.4 p.u. is emulated, which still provides a certain fundamental frequency circulating current in the conventional arm energy balancing control. As a result, the SM capacitor voltages between upper and lower arms can be balanced.

In Fig. 14(b), a more severe fault is reproduced with fault depth D=0.95. The transient fault current I_{pcc_max} and continuous overcurrent I_{pcc_lim} injected by the DUT are constrained as 1.5 p.u. It is clear that the fault current and a low residual PCC voltage 0.05 p.u. weaken the efficacy of conventional energy balancing control, leading to transient overvoltage and continuous voltage imbalance in SM capacitors.

In Fig. 14(c), the influence of transient fault current injection on SM capacitor voltages is evaluated. Compared to Fig. 14(b), I_{pcc_lim}=1.5 p.u. and D=0.95 lead to the same SM capacitor voltage ripple, i.e., 0.15 p.u. during emulated grid fault. However, a higher transient fault current I_{pcc_max}=2 p.u. increases dc voltage changes in SM capacitors after t_{sag}, leading to more severe transient overvoltage (1.17 p.u.) and voltage imbalances. Hence, both I_{pcc_max} and I_{pcc_lim} contribute to the transient SM capacitor overvoltage.

Fig. 15 illustrates the CHIL result for the MMC-based GE using the enhanced EBC during a FRT test. When the PCC voltage sags, switching to a lower k_n can reduce the averaged voltage of SM capacitors to mitigate their overvoltage. Injecting i_{cirj_ac} through the designed signal $K_{in}\cos(\omega_1 t+\theta_{inj})$ effectively mitigates voltage imbalances in upper- and lower-arm SM capacitors.

5.4 Mitigation of transformer saturation for converter-based GEs [J4] [C3]

This work first evaluates the issues of the traditional anti-saturation control (ASC) in mitigating transformer saturation. It is found that the traditional ASC tends to distort the PCC voltage or even interact with the output VC of GEs, causing transformer flux oscillations. An adaptive ASC solution is then introduced to alleviate the transformer saturation with lower PCC voltage distortion. Further, the adaptive ASC effectively alleviates its interaction with the VC when emulating voltage steps at the PCC.

1) System Description

Fig. 16 shows the converter-based GE using a general ASC. v_{1j} (i_{1j}) and v_{pccj} (i_{pccj}) are the primary-side and secondary-side voltage (winding current) of the GE transformer, respectively. *j* denotes phase *a*, *b* or *c*. λ_j is the each-phase transformer flux. For the transient flux control (TFC), R_{tfc} denotes the virtual resistance

activated when the estimated flux surpasses the preset flux threshold λ_{th}. In the steady-state flux control (SFC), the notch filter and the low-pass filter (LPF) or moving average filter (MAF) are typically used to extract the dc offset in the estimated flux. Additionally, v_{mj}^* denotes the sinusoidal modulation reference, which is formulated

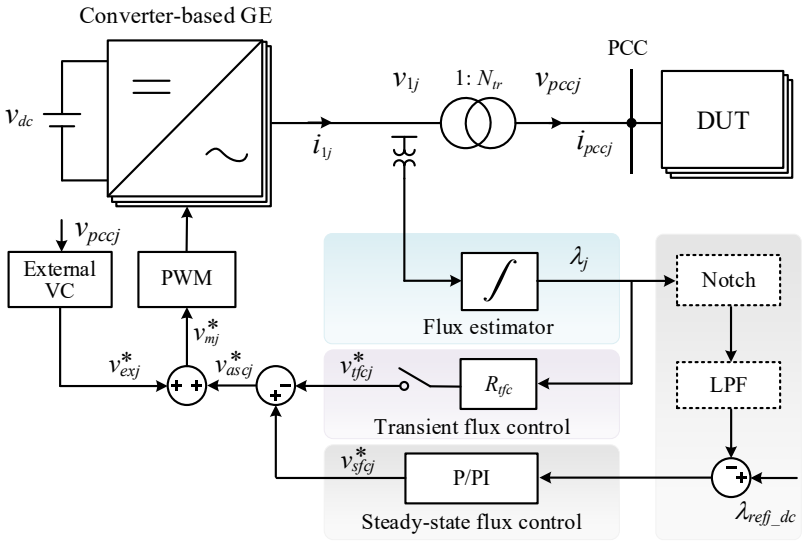


Fig. 16 Diagram of the converter-based GE using a general ASC [J4].

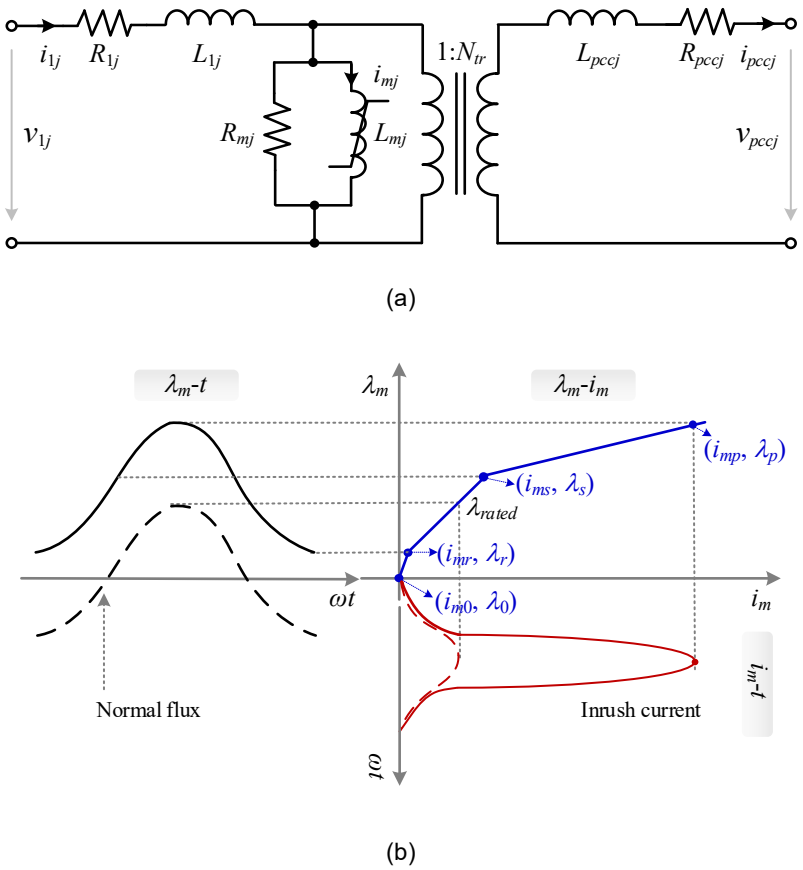


Fig. 17 Model and characteristics of the GE transformer. (a) Single-line model. (b) Magnetic characteristics [J4].

by superimposing the output commands of the VC (v^*_{exj}) and the ASC (v^*_{ascj}).

Fig. 17(a) depicts a single-line transformer model. R_{1j} (R_{pccj}) and L_{1j} (L_{pccj}) denote the primary-side (PCC-side) leakage resistance and inductance, respectively. R_{mj}, L_{mj}, i_{mj} and λ_{mj} denote the core-loss resistance, magnetizing inductance, magnetizing current and magnetic flux, respectively. Fig. 17(b) depicts the magnetic characteristics of the GE transformer, where (i_{m0}, λ_0), (i_{mr}, λ_r), (i_{ms}, λ_s) and (i_{mp}, λ_p) are four critical points. λ_0, λ_r, λ_s and λ_p represent the initial flux, the residual flux, the saturation flux and the maximum flux, respectively. i_{m0}, i_{mr}, i_{ms} and i_{mp} are corresponding magnetizing currents. Typically, λ_j is able to be a sinusoidal signal without dc offset in the normal operation. However, during grid fault emulation, the steps with both magnitude and phase angle of the PCC voltage potentially introduce an extra dc flux λ_{j_dc} into λ_j, particularly after fault clearance. When the magnitude of post-fault flux $|\lambda_{ptj}|$ is larger than λ_s, the transformer is saturated, causing a significant inrush current, as illustrated in Fig. 17(b). Therefore, the ASC is typically used in GEs to shape v_{1j} and v_{1fj} for counteracting λ_{j_dc}, thereby mitigating transformer saturation.

2) Problem statement

- PCC voltage distortion: According to grid-code requirements, the allowed tolerance of the reproduced steady-state PCC voltage should be within 5% of the rated voltage. Thus, the output command of SFC is commonly limited within ±0.05 p.u., a value deemed negligible compared to the contribution of TFC on the ASC. Fig. 18 depicts the PCC voltage distortion when enabling the traditional TFC after clearing the emulated grid fault. When $|\lambda_{ptj}|>\lambda_{th}$, the TFC generates $R_{tfc}\lambda_j$, which induces a significant distortion in v_{pccj}, deviating from its initial reference, i.e., the dashed line in Fig. 18.

- Interaction between traditional ASC and VC: Fig. 19 illustrates the small-signal model for the GE utilizing

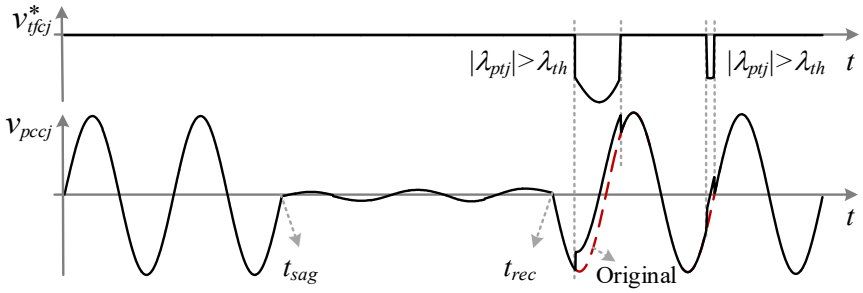


Fig. 18 Impact of the traditional TFC on PCC voltage distortion [J4].

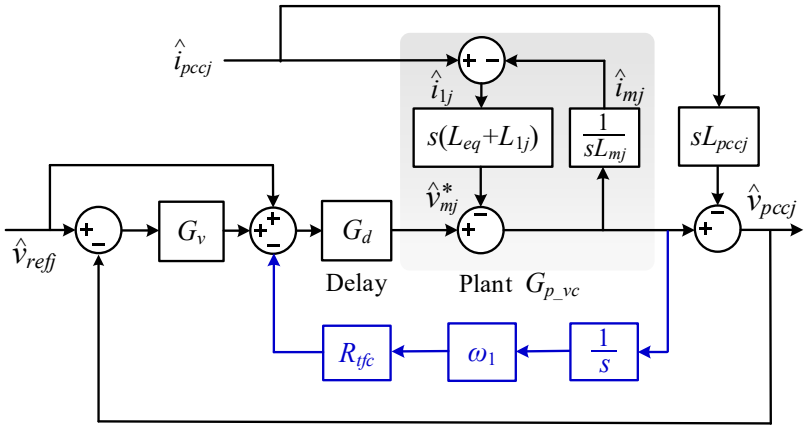


Fig. 19 Small-signal model of the GE using a closed-loop VC and the traditional ASC [J4].

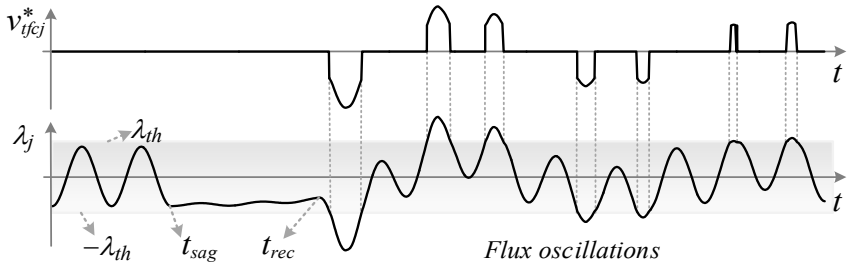


Fig. 20 Transient flux oscillations induced by the interaction between the traditional ASC and the VC [J4].

a closed-loop VC and the traditional ASC. Through this modeling analysis, it is found that the interaction between VC and traditional ASC reduces the damping provision of the traditional FC, which tends to cause transformer flux oscillations. Fig. 20 shows the transient flux oscillations resulting from the interactive effect between the traditional ASC and the VC. This interaction induces insufficient damping of the ASC, causing an extended settling time of the transformer flux regulation. If the settling time surpasses one fundamental-frequency cycle, activating a low-damped R_{tfc} in each cycle may give rise to transient flux oscillations or even cause instability issues.

3) Enhanced control method

Fig. 21 shows the block diagram of the adaptive ASC and the VC. The transformer flux is estimated through the integral of v^*_{mj} to avoid utilizing extra voltage sensors at the primary side of the GE transformer. The SFC incorporates a MAF and a proportional-integral (PI) controller to mitigate the continuous dc flux, while the TFC utilizes a virtual adaptive resistor R_{tfcj}, proportional to λ_j, to alleviate the transient inrush current during transformer saturation. Besides, the output v^*_{ascj} of the ASC is overlayed to both the modulation reference and the VC reference to alleviate the interactive effect between the adaptive ASC and the VC.

Fig. 22 depicts the diagram for calculating R_{tfcj}. To obtain the magnitude of the per-phase flux λ_{estj_mag}, a $T/4$ delay (5 ms for a 50 Hz-grid) is applied to generate a fictitious quadrature flux λ_{estj_β}. Here, λ_{estj} can be seen as

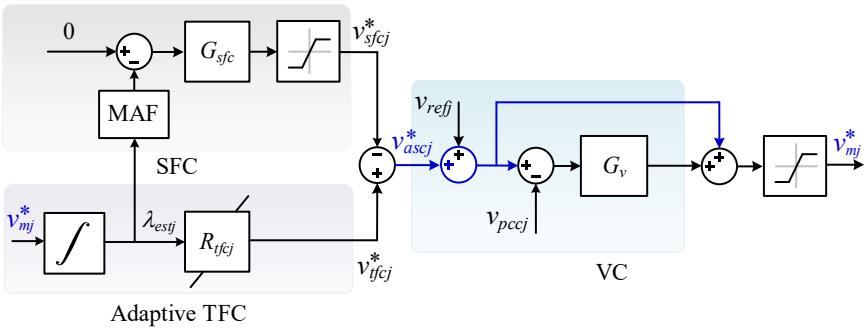


Fig. 21 Diagram for the adaptive ASC and the VC [J4].

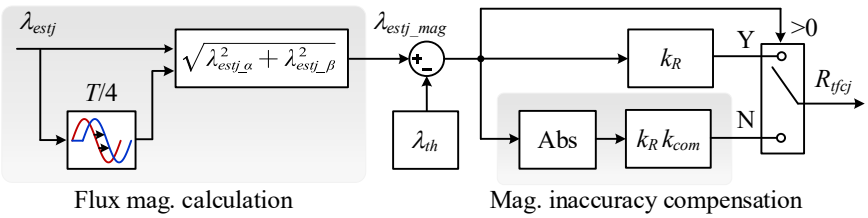


Fig. 22 Diagram for calculating R_{tfcj} [J4].

the α-axis signal. Yet, the delay block introduces an inaccuracy in the flux magnitude calculation, which may postpone the activation of the adaptive TFC, limiting its transient dynamics. Thus, a compensation block is introduced to counteract the adverse influence of the $T/4$ delay. Specific equation and design guideline for R_{tfcj} can be found in [J4].

4) CHIL validation

Fig. 23 depicts a CHIL testing platform established by two RT Boxes. A FBSM-based MMC featuring three single-phase transformers are used in the GE. The control strategies of the GE are distributed within the lower RT Box. Additionally, the main circuit of the GE and the overall DUT system are simulated within the upper RT Box.

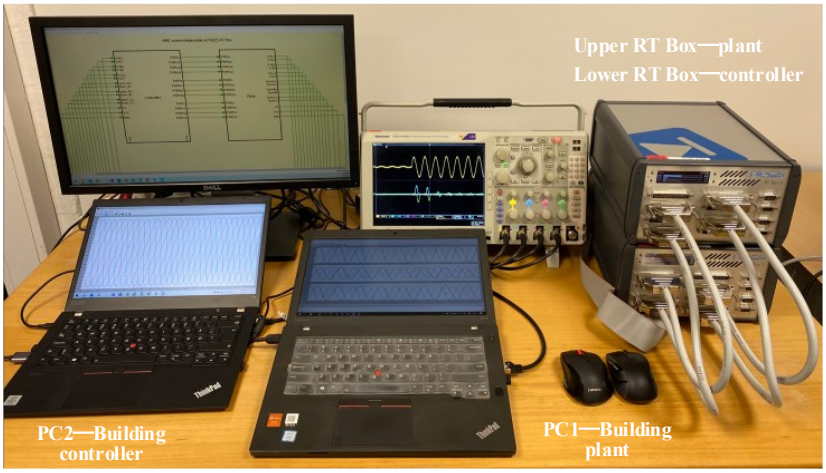


Fig. 23 CHIL testing platform [J4].

Fig. 24 shows the specific distribution of control algorithms and main circuits for the MMC-based grid emulation system in dual RT Boxes. The DUT is a general GFL WT inverter and its averaged model is used for simplicity. Due to the limited number of I/Os, the GFL control of the DUT is implemented in the upper RT Box. The current reference for the DUT is provided by the lower RT Box. Here, "I_{d_ref}" denotes its d-axis current reference, while "En_GC" is the enable signal for switching to the current reference required by grid codes. Additionally, the lower RT Box serves as the digital controller for the MMC-based GE, implementing the analog signal processing, the external VC, the internal EBC, the adaptive ASC and the PSC-PWM.

Fig. 25 demonstrates the adverse impact of control interaction between the conventional flux control and the closed-loop VC. In Fig. 25(a), without the ASC, the transformer experiences saturation with an inrush current up to 4.2 p.u. during the fault recovery process, which would trip the GE in practice. In Fig. 25(b), although using the conventional ASC can alleviate a certain of transient inrush current, it interacts with VC, leading to low-frequency flux oscillations. In Fig. 25(c), increasing the proportional gain K_{pv} of the VC can dampen the oscillations, but the transient inrush current still reaches up to 2.8 p.u..

Fig. 26 depicts the CHIL results for the MMC-based GE using the adaptive ASC with the VC and K_{pv}=0.1 p.u.. As the critical coefficient k_R of the virtual resistance introduced by the adaptive ASC increases, this control enhances the mitigation of transient inrush current, but it also induces more severe distortion in the PCC voltage. Consequently, a compromised k_R=1.3 is adopted, which is consistent with the theoretical analysis in [J4].

Fig. 27 demonstrates the feasibility of the adaptive ASC with kR=1.3 in the GE considering the DUT connection. Three scenarios are successfully reproduced, i.e., the balanced fault without phase jump, the balanced fault with phase jump and the line-to-line fault including the simultaneous voltage sag and phase jump.

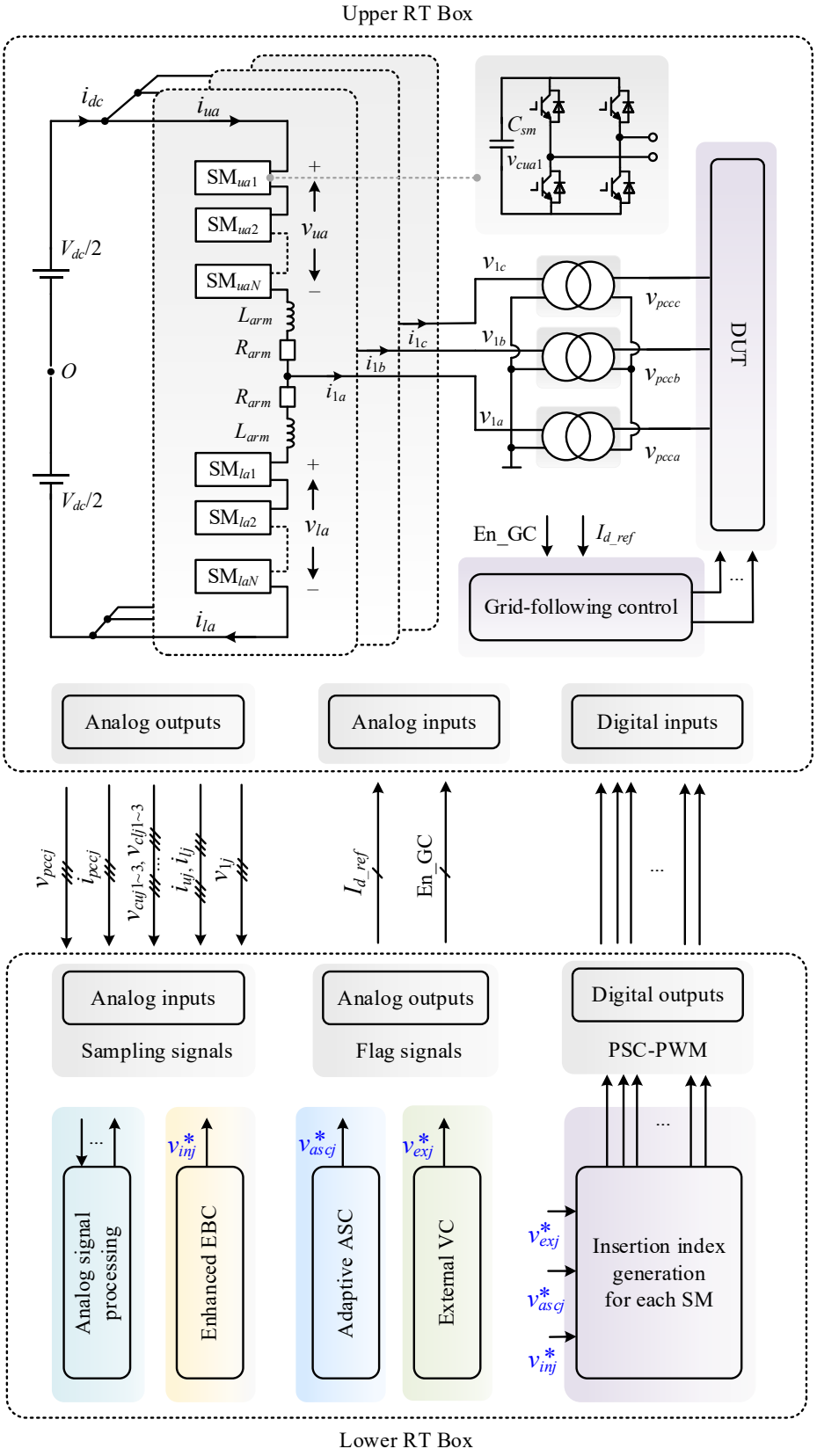
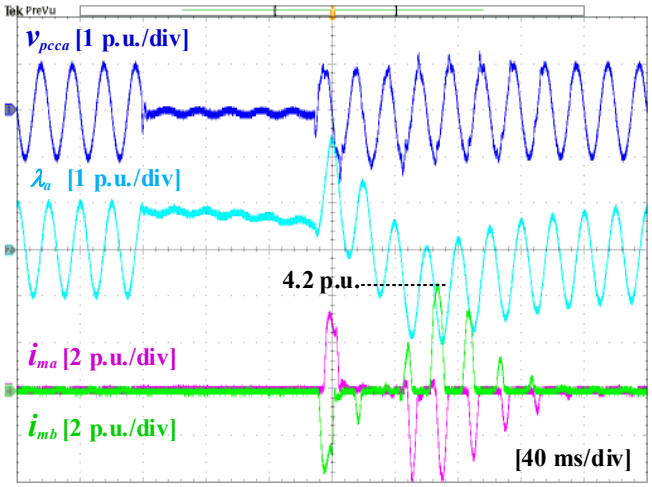
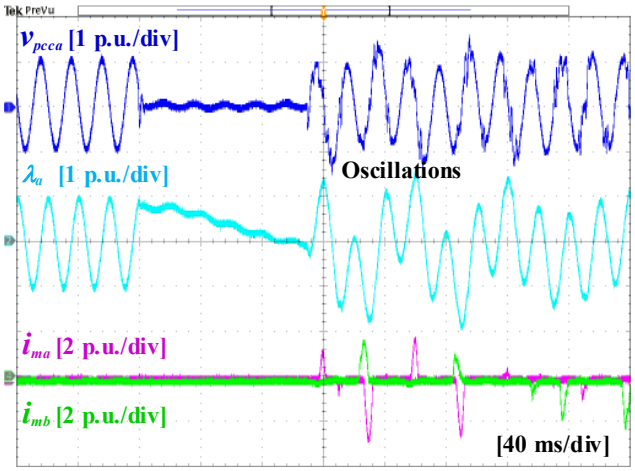


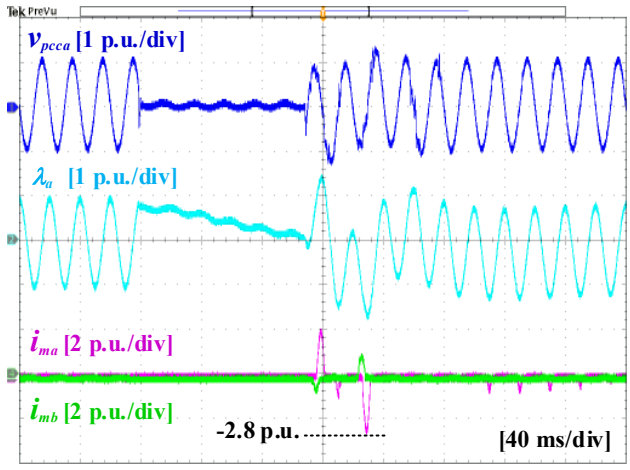
Fig. 24 Distribution of control algorithms and main circuits in RT Boxes [T1].



(a)

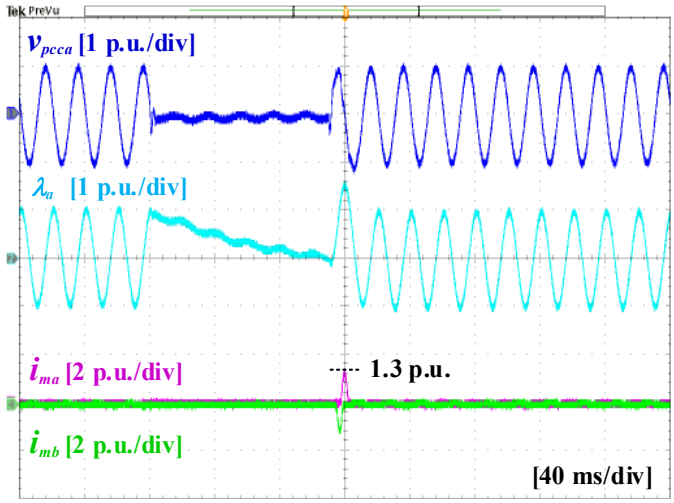


(b)

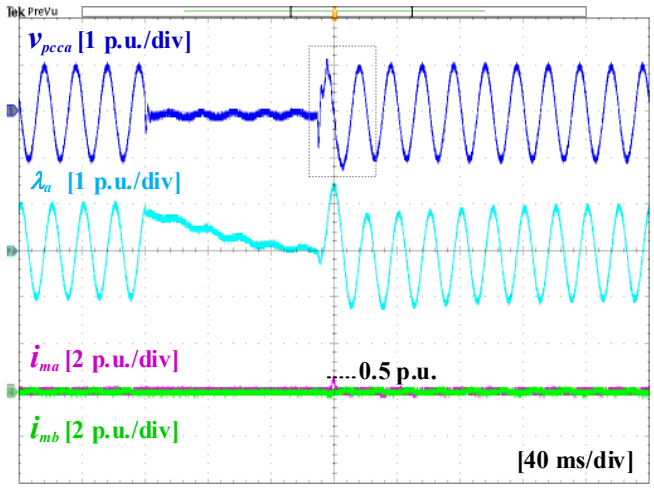


(c)

Fig. 25 Results for the GE utilizing a closed-loop VC with or without ASC. (a) Without ASC (K_{pv}=0.1 p.u.). (b) Using the conventional ASC (K_{pv}=0.1 p.u., R_{tfc}=0.65 p.u.). (c) Using the conventional ASC (K_{pv}=0.7 p.u., R_{tfc}=0.65 p.u.).

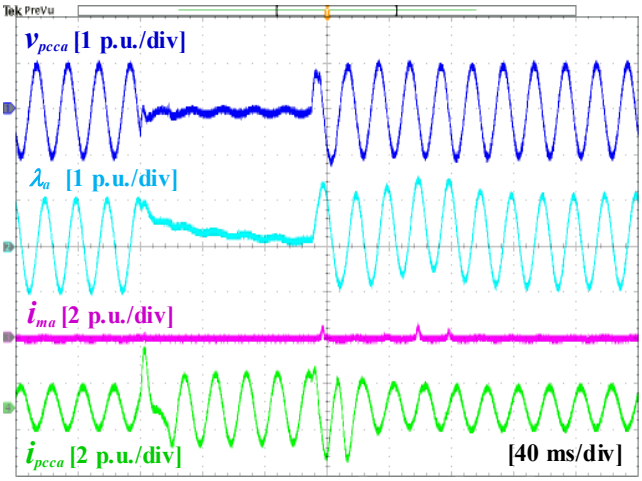


(a)

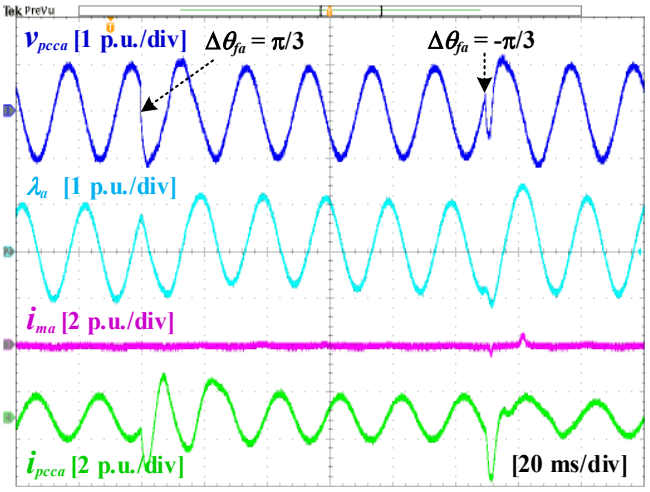


(b)

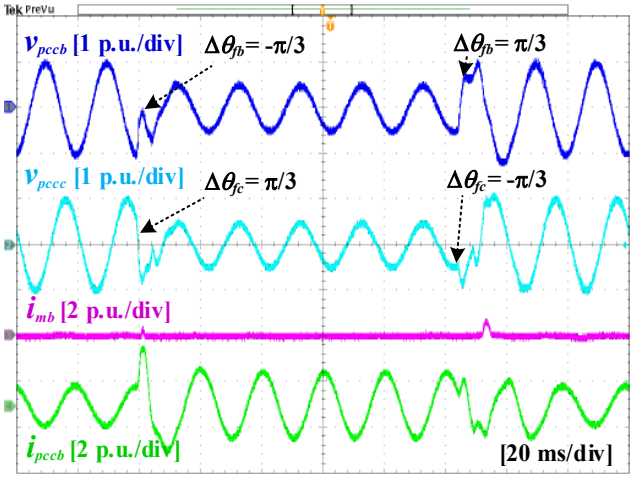
Fig. 26 Results for the proposed ASC-controlled GE and K_{pv}=0.1 p.u.. (a) k_R=0.3 p.u.. (b) k_R=1.3 p.u..



(a)



(b)



(c)

Fig. 27 Results for the proposed ASC-controlled GE interfacing with the DUT. (a) Balanced fault w/o phase jump (D=0.98, $\Delta\theta_{fj}$=0). (b) Balanced fault w/ phase jump (D=0.05, $\Delta\theta_{fj}$=π/3). (c) Phase-*b to* Phase-*c* fault (D=1, $\Delta\theta_{fj}$ =π/3).

5.5 Co-design of voltage and impedance control for impedance emulation [C4] [C5] [T1]

The voltage changes are often accompanied with the impedance variations in real grid faults, which may be detrimental to the dynamic performance of DUTs, leading to transient overvoltage or even low-frequency (<100 Hz) oscillations. To reproduce such grid events, the external impedance control for the MMC-based GE is needed. This work reveals that the virtual admittance (VA) control can improve the accuracy of emulating steady-state impedance in the low-frequency range and transiently varying impedance, while it may induce internal instability when interacting with its inner current control (CC) loop. Moreover, the time delay in the VA loop can introduce the high-frequency negative resistance (-R) in the emulated impedance. A passivity-based co-design method of the VA and CC is thus proposed. It can synthesize accurate low-frequency impedance, and meanwhile, reducing the risk of high-frequency instability, thereby reproducing the overvoltage and voltage oscillations at the PCC.

1) System Description

Fig. 28 illustrates the general diagram of the MMC-based GE and outlines the principle of synthesizing grid impedance. In Fig. 28(a), the GE is equivalent as a controlled voltage source behind a programmable impedance, aiming to emulate simultaneous changes in the PCC voltage and grid impedance during grid faults. Conventionally, this objective is achieved by the shunt-impedance-based GE, as shown in Fig. 28(b). Z_{gj}, Z_{1j} and Z_{2j} are the grid impedance, series impedance and fault impedance, respectively. Fig. 28(c) depicts the time sequence of impedance variations during grid fault emulation. AEMO imposes that the SCR of the emulated grid in the pre-fault and post-fault processes should be able to be as low as 1.5 and the X/R ratio of Z_{gj}, Z_{1j} and Z_{2j} must be at least 2. Although this requirement can be realized by a shunt-impedance-based GE, it leads to extensive energy loss, particularly for testing a high-power DUT. Therefore, the MMC-based GE should be able to follow the principle, as shown in Fig. 28(c), to replace the traditional shunt-impedance-based GE.

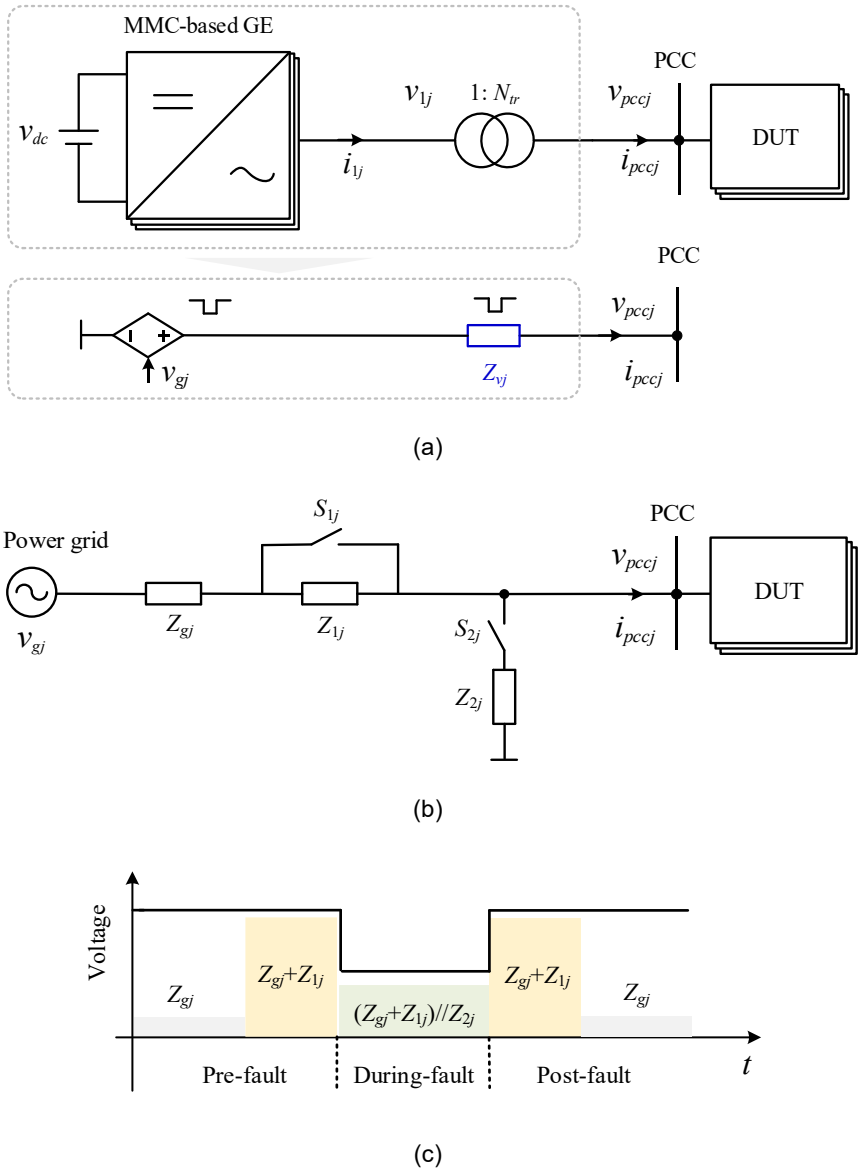


Fig. 28 General diagram of the MMC-based GE and the principle of grid impedance emulation. (a) MMC-based GE. (b) Shunt-impedance-based GE. (c) Time sequence of impedance changes [C4] [T1].

2) Problem statement

There are two typical control methods for grid impedance emulation, i.e., 1) the VC and virtual impedance (VI) control and 2) the CC and VA control. The effectiveness and issues of synthesizing the required impedance by VI and VA controls are discussed as follows.

- VC and VI control:

Fig. 29 illustrates the small-signal model of the GE using the VC and VI control in the $\alpha\beta$-frame. Z_{op}=sL_{eq}+R_{eq} and Z_v=sL_v+R_v denote the open-loop impedance and the emulated impedance, respectively. L_{eq} and R_{eq} denote the equivalent inductance and resistance of the arm filter and the GE transformer, respectively. R_v and L_v denote the emulated resistance and inductance, while G_v and G_d are the transfer functions for the PR controller and the time delay link, respectively. H represents a LPF employed to mitigate the sampling noise amplification resulting from the derivative term "s" in Z_v.

Based on the model in Fig. 29, Fig. 30 shows the bode diagrams of output impedance Z_{GE} and the ideal impedance Z_{ideal}. From Z_v=0.02 p.u. to Z_v=0.67 p.u., a large mismatch between Z_{GE} and Z_{ideal} within the low-frequency range exists even using K_{pv}=0.7. Besides, as Z_v decreases, the -R of Z_{GE} appears within the frequency range [f_1, 1/(4T_d)], which is dependent on the time delay, control plant and LPF. If the output impedance of a DUT also exhibits -R within [f_1, 1/(4T_d)], the interaction between the GE and the DUT may lead to harmonic instability [C3].

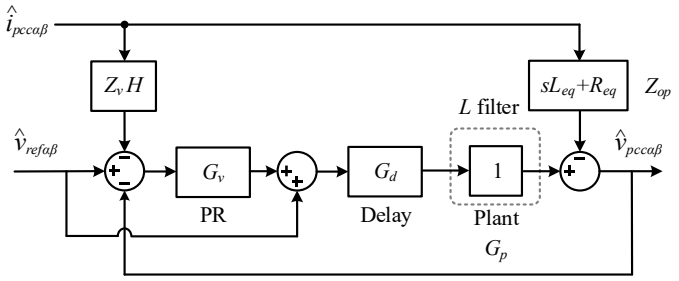


Fig. 29 Small-signal model with the VC and VI control [C4].

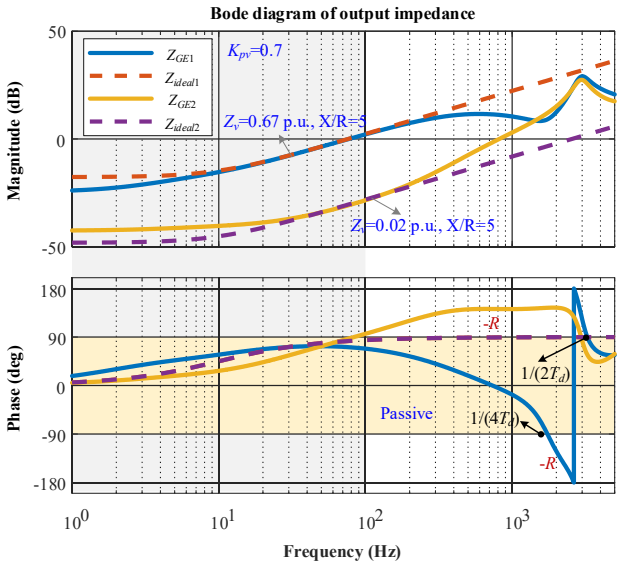


Fig. 30 Bode diagram of Z_{GE} and Z_{ideal} for the GE when utilizing the VC and VI control [C4].

- CC and VA control:

Fig. 31 illustrates the small-signal model of the GE using the CC and VA control. Y_v and G_i denote the transfer

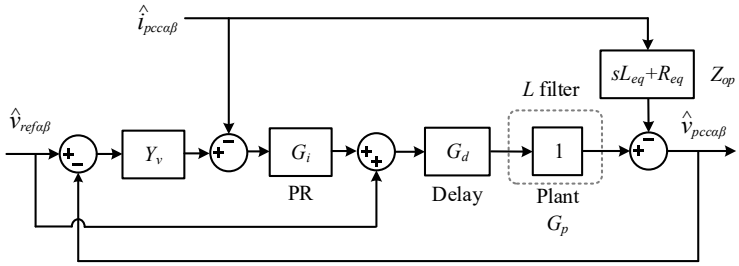
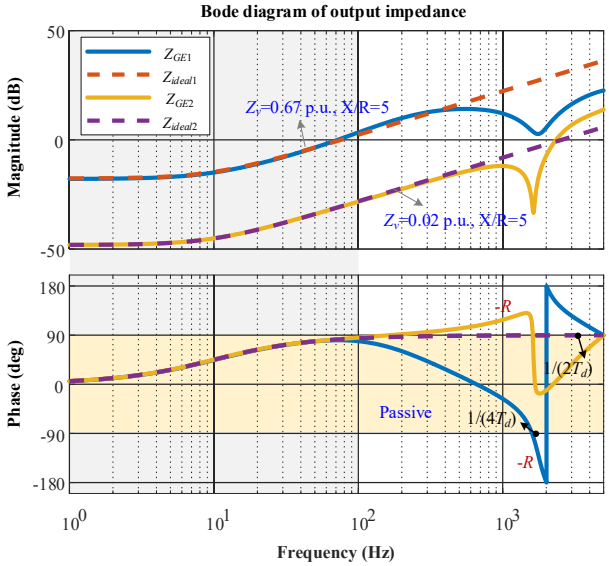
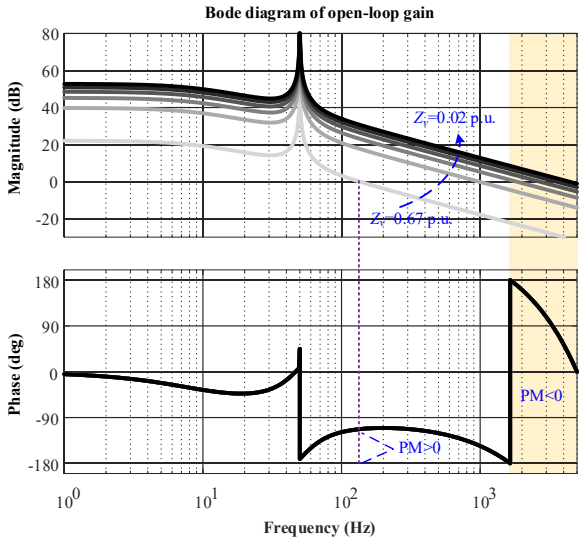


Fig. 31 Small-signal model with the CC and VA control [C4].



(a)



(b)

Fig. 32 Bode diagrams of Z_{GE}, Z_{ideal} and open-loop gain G_{opva} for the GE when using the CC and VA control. (a) Z_{GE} and Z_{ideal}. (b) G_{opva} for the GE using constant K_{pc} and K_{rc} with different Z_v. [C4].

functions of the VA and proportional-resonant (PR) controller of the CC, respectively. Based on the model, Fig. 32 shows the bode diagrams of Z_{GE}, Z_{ideal} and the open-loop gain G_{opva} for the GE when using the CC and VA control. In Fig. 32(a), from Z_v=0.02 p.u. to Z_v=0.67 p.u., the VA control maintains high accuracy of the emulated impedance in the low-frequency region. However, the $-R$ within [f_1, $1/(4T_d)$] appears as Z_v decreases. In Fig. 32(b), with constant proportional gain K_{pc} and the resonant gain K_{rc}, the CC significantly interacts with the VA control when emulating a small impedance, which may lead to a negative PM of G_{opva}, causing internal instability of the GE.

Considering the limitation of LPF and the low-frequency mismatch in the emulated impedance when using the VI control, this project focuses on enhancing the CC and VA control.

3) Enhanced control method

[T1] provides the specific design guideline for the enhanced co-design method of the CC and VA control. The proportional gain K_{pc} and the resonant gain K_{rc} of the CC are proportional to the emulated inductance, i.e., $K_{pc}=\pi L_v/(4T_d)$. Moreover, considering the mitigation of negative resistance and internal stability, the upper and lower limits of K_{pc} and K_{rc} are identified. For more details, please see [T1]. Fig. 33 shows the bode diagram of Z_{GE} when using $K_{pc}=\pi L_v/(4T_d)$ with its limits. It eliminates $-R$ in the resistive-capacitive impedance and mitigates overlarge $-R$ in the resistive-inductive impedance.

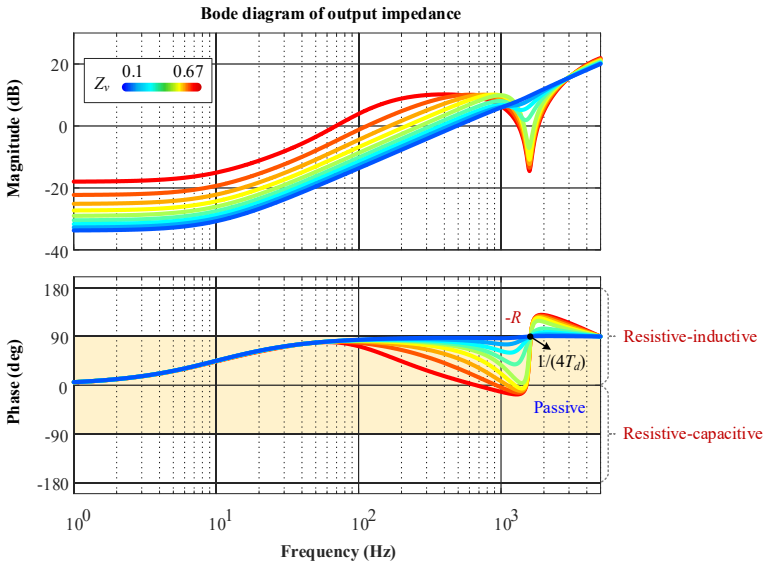


Fig. 33 Bode diagram of Z_{GE} when using K_{pc} varying to L_v and its upper limit.

4) CHIL validation

To validate the effectiveness of synthesizing grid impedance during fault emulation, both the MMC-based and the shunt-impedance-based grid emulation systems are simultaneously implemented in the CHIL setup. Fig. 34 shows the specific distribution of control algorithms and circuits for the two testing systems. In the upper RT Box, the same GFL control scheme and parameters are used in DUT 1 and DUT 2, which are connected to the MMC-based and shunt-impedance-based GEs, respectively. Besides setting "I_{d_ref}" and "En_GC" signals for two DUTs, the lower RT Box generates "En_GE_S" and "Active_Falut" flag signals to configure the shunt-impedance-based GE. "En_GE_S" is the synchronization signal to simultaneously enable the MMC-based and shunt-impedance-based GEs. "Active_Falut" is the enable signal for the grid fault emulation.

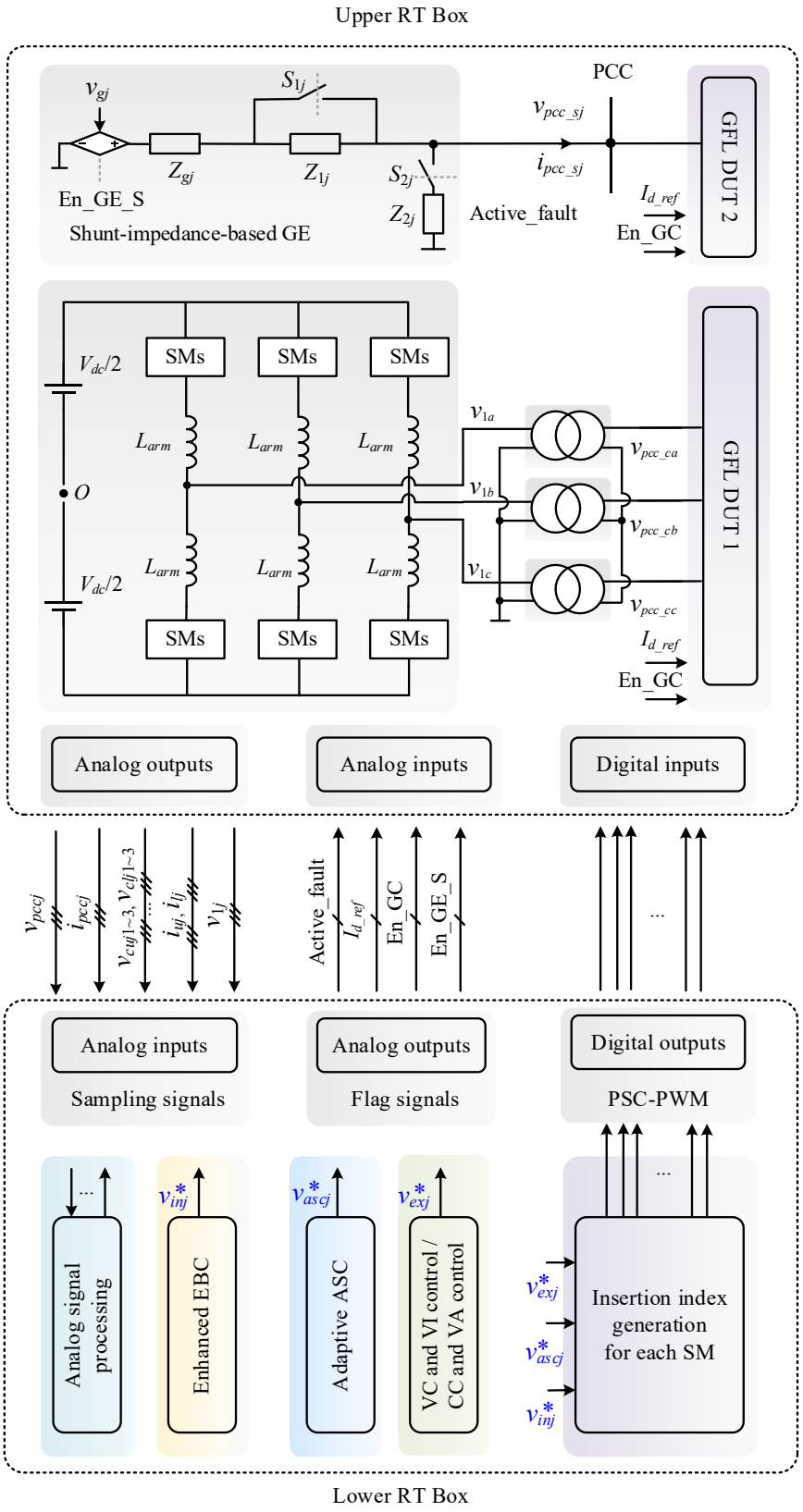


Fig. 34 Distribution of control algorithms and circuits for two testing systems.

Figs. 35-36 show comparative results of the shunt-impedance-based GE and the MMC-based GE without considering transformer saturation. C1 (v_{pcc_sa}) and C2 (i_{pcc_sa}) denote the phase-*a* PCC voltage and current for the shunt-impedance-based GE, respectively. C1 (v_{pcc_ca}) and C2 (i_{pcc_ca}) denote the phase-*a* PCC voltage and current for the MMC-based GE, respectively.

Fig. 35 shows the CHIL results for the GE using the conventional VC and VI control. Taking the post-fault grid impedance Z_{ideal}=0.5 p.u. (SCR=2) as an example, a DUT should interact with the weak grid, leading to original PCC overvoltage and low-frequency oscillations. However, it is clear that, compared to the shunt-impedance-based GE, the MMC-based GE using the VC and VI control dampens the original voltage oscillations in the post-fault process.

Fig. 36 shows the CHIL results for the GE using the conventional CC and VA control. In Fig. 36(a), when using the same CC parameter for emulating both Z_v=0.02 p.u. and Z_v=0.5 p.u., the internal instability occurs in the GE during the in-fault process. In Fig. 36(b), by reducing CC parameters for Z_v=0.02 p.u. emulation, the internal instability issue is addressed. However, the ideal PR controller cannot realize accurate tracking for the low-frequency oscillations. As a result, the oscillating frequencies in the MMC-based GE diverge, differing from those in the shunt-impedance-based GE system.

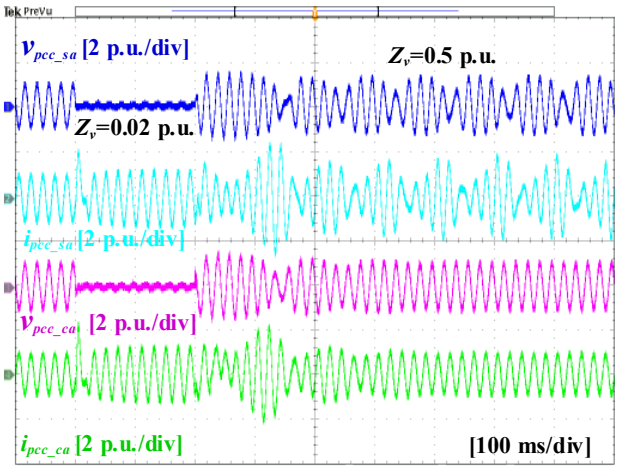
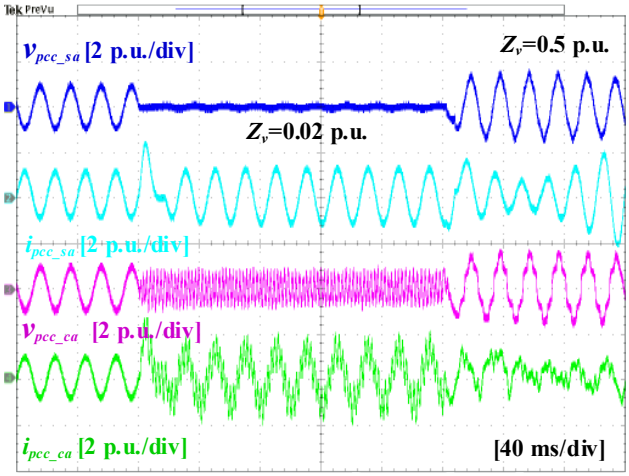
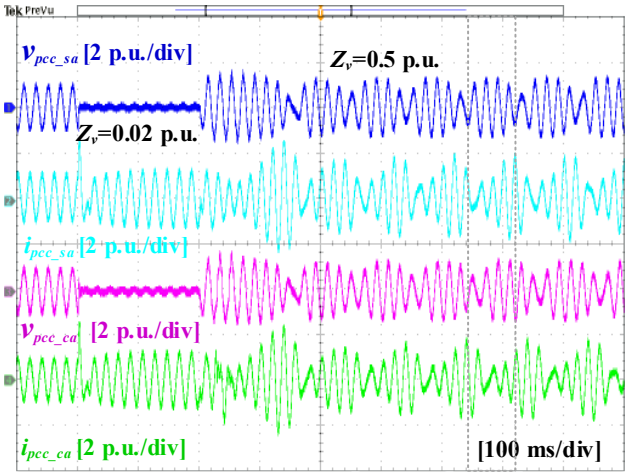


Fig. 35 CHIL results for the GE using the conventional VC and VI control.

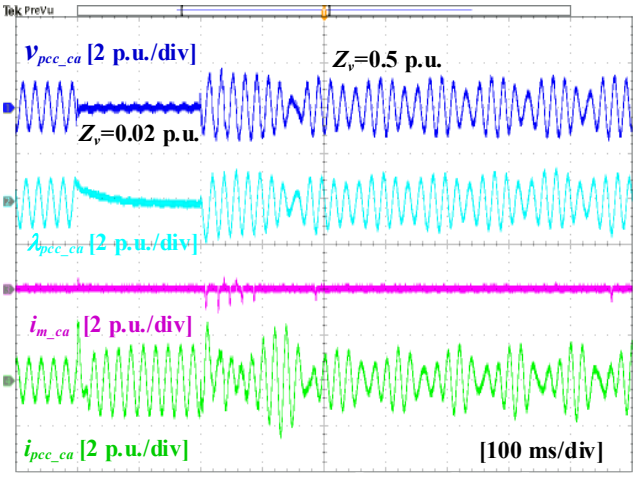


(a)

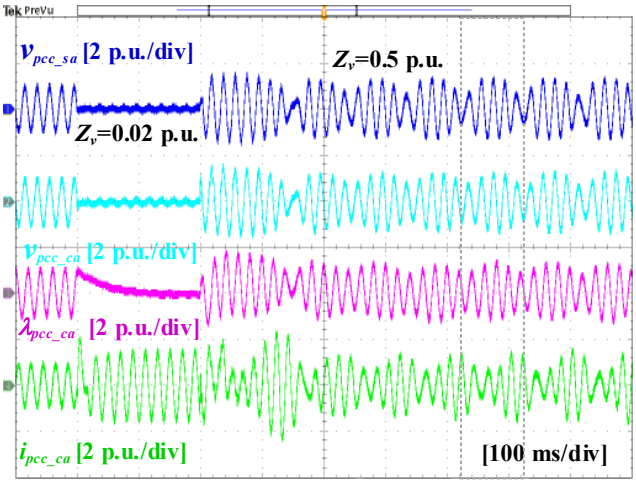


(b)

Fig. 36 CHIL results for the GE using the conventional CC and VA control. (a) Internal instability. (b) Oscillating frequency different from the shunt-impedance-based grid emulation system.



(a)



(b)

Fig. 37 CHIL results for the MMC-based GE using the proposed CC and VA control considering the impact of transformer saturation. (a) Inrush current in the MMC-based GE. (b) Comparison of both GE systems.

Fig. 37 depicts CHIL results for the MMC-based GE using the proposed CC and VA control considering the impact of transformer saturation. In Fig. 37(a), the transient PCC overvoltage worsens transformer saturation during fault recovery, which leads to transient inrush current even though using the adaptive ASC in this period. For the low-frequency oscillations, the adaptive ASC is not activated when the transformer flux is lower than the saturation flux, which exhibits a minor influence on the PCC dynamics. In Fig. 37(b), after using the enhanced CC controller, v_{pcc_ca} matches with v_{pcc_sa}, indicating that the MMC-based GE can accurately reproduce the transient PCC overvoltage and low-frequency oscillations. Moreover, the influence of transformer saturation on the reproduced grid impedance can be disregarded for simplicity when using the adaptive ASC.

Most of the aforementioned technical accomplishments were outlined in the project proposal. The development of the adaptive ASC method came as a significant surprise. This method emerged from a collaborative effort between our team and Fraunhofer Institute for Wind Energy Systems (IWES), facilitated by a study abroad program undertaken by a PhD student Zejie Li at AAU.

Commercial results

R&D Test systems was able to secure their first ever grid emulator order in the last year of the project. Even though it was quite a small project, it was a huge achievement for the project. It proves that the knowledge gained from MERGE and related projects can be used commercially, and it could kick start the practical experience and track record of the team at R&D Test Systems, so show other potential customers their capabilities and expertise.

The realization that R&D should not be a hardware manufacturer and try competing with other well established production companies who has optimized their supply chain and manufacturing processes through years and years, is also an extremely valuable outcome of the project.

Furthermore the numerous conversations that has evolved around R&D trying to get into the grid emulator market during the MERGE project has extended the network and established connections to many possible future customers, and the dissemination of the results from the MERGE project has helped both R&D and AAU to become much more know as expert in the grid emulation field.

6. Utilisation of project results

Future use of the results

The identified design considerations, latest testing capabilities, dynamic challenges, and control solutions will guide the development of power/control hardware and control algorithms for the practical megawatt grid emulators currently under construction.

The proposed internal SM energy balancing control has potential applications in future megawatt MMC-based GEs developed by R&D Test Systems.

The proposed adaptive ASC, external voltage, and impedance control schemes are feasible for application in megawatt GEs worldwide, including institutions such as Fraunhofer IWES, National Renewable Energy Laboratory (NREL), Lindø Offshore Renewables Center (LORC), Aachen University, and others.

Commercial use of the results

In the time between the kick-off of MERGE and now, R&D has created and developed a new important business leg called “Digital solutions” This department evolves around digitalizing the test systems with advanced simulations, digital twins, hybrid testing. Together with the High voltage department, this could open new markets where R&D has an edge with their deep knowledge within large scale digitalized test systems.

So far, the project has only increased the turnover of R&D Test Systems by a very small amount. It has become clear within the project that in addition to a very high entry level knowledge-wise, the marked is led by repurchases from existing customers, due to the high risks involved in such projects, and the fact that hardware from the same suppliers can be easier to integrate into existing systems. This is also why R&D expects that the most accessible sales channels will be selling grid emulators as an add-on to large scale test benches for generators and drive trains.

Contribution to realisation of energy policy objectives

Megawatt GEs provide promising approaches to emulate power grid faults and test the grid-code compliance of renewable energy resources, such as wind and solar. By guaranteeing the reliability and stability of renewable energy integration into the power grid, these emulators contribute to realise energy policy objectives focused on enhancing grid resilience and reducing the risk of blackouts. Moreover, they can further increase the potential capacity of renewable energy in the power grid, thereby reducing reliance on fossil fuels and mitigating climate change.

Ph.D.’s teaching and other dissemination activities.

The project doesn't yield any outcomes applicable for teaching purposes. However, it does cover the overlength fee and open-access fee for the journal papers mentioned above. Additionally, it includes support for the registration fee and travel expenses for international conferences attended by a PhD student Zejie Li.

7. Project conclusion and perspective

Conclusion

This project has first investigated the topology comparison, power hardware design considerations, latest testing capability requirements, dynamics challenges of megawatt converter-based GEs. Further, analytical models and enhanced control schemes are developed to evaluate and address identified dynamics challenges. The specific conclusions are outlined as follows.

1. Overview of Topologies and Power Hardware Design: This study points out that the GE technology is evolving toward high scalability and filter-less design for versatile testing of energy renewable resources. The MMC-based GE is identified as an attractive solution for future medium/high voltage (66 kV~132 kV) testing applications. Design considerations of power components in GEs have also presented, such as the oversized design of power semiconductor devices, the selection of

the number of SMs, SM capacitance, arm inductance, dc-link choppers, the anti-saturation design of transformers, and the double insulation of switchgear.

2. Overview of Testing Capabilities and Dynamics Challenges: Based on the recent development of grid codes and standards, the latest testing capability requirements have been identified for GEs, which mainly involve five dimensions: emulating voltage sags and swells, synthesizing grid impedance, generating flickers and harmonic voltage, reproducing grid frequency deviation, and the provision of these testing capabilities simultaneously. When implementing these testing capabilities, the MMC-based GE may encounter three typical dynamics challenges, i.e., 1) the transient overvoltage and voltage imbalances in SM capacitors, 2) the transformer saturation, and 3) the adverse interaction between the GE and a DUT when emulating grid impedance and harmonic voltage.

3. Mitigation of Overvoltage and Voltage Imbalances in SM Capacitors: When the MMC-based GE reproduces severe voltage sags, changes in the PCC voltage and the fault current injected by a DUT tend to cause transient overvoltage and voltage imbalances in SM capacitors. To mitigate transient overvoltage, the enhanced phase energy balancing control incorporates a reasonable scaling factor of the energy sum of SM capacitors per phase, which ensures capacitor voltages within 70%~110% of the normal value and avoids excessive capacitor voltage ripple. To mitigate voltage imbalances, the enhanced arm energy balancing control injects a specific fundamental-frequency circulating current, which effectively balances the upper- and lower-arm SM capacitor voltages, even when the emulated PCC voltage is nearly zero.

4. Mitigation of Transformer Saturation: When emulating voltage steps, the ASC is required for the converter-based GE to actively mitigate the inrush current caused by the transformer saturation. It is found that the conventional ASC may distort the PCC voltage and even interact with the voltage control of the GE, leading to transformer flux oscillations. An adaptive ASC solution is then introduced to alleviate the transformer saturation with lower PCC voltage distortion. Further, the adaptive ASC effectively alleviates its interaction with the voltage control when emulating voltage steps at the PCC.

5. Mitigation of Interaction Between GE and DUT: When reproducing grid impedance and voltage, the time delay of the converter-based GE may introduce negative resistance into the output impedance, which adversely interacts with control dynamics of DUT, potentially leading to instability issues. The passivity-based design of voltage control, active damping control and impedance control are proposed in this project to mitigate the negative resistance, enhancing the voltage and impedance dynamics at the PCC.

Next steps

1. Experimental Validation in Field Tests: Conducting experimental validation of the proposed control schemes in megawatt scenarios to verify their effectiveness and refine them further based on practical insights gained from real-world testing.

2. Knowledge Exchange: Engaging stakeholders, including industry engineers and academic researchers, in discussions about the benefits and capabilities of the developed technology through workshops, seminars, and publications, fostering collaboration and disseminating valuable insights.

3. Scaling and Commercialization: Applying the developed technology for broader applications and enhancing its potential for commercialization. This may involve collaboration with industry partners like R&D Test Systems to integrate the developed solutions into their products or systems, facilitating wider adoption and market penetration.

Perspective

1. Standardization and Industry Adoption: The insights into testing capability requirements and dynamics challenges of Grid Emulators (GEs) can drive standardization efforts within the industry. By developing standardized solutions based on these findings, the adoption of GE technologies can be facilitated across various applications, ensuring compatibility and interoperability.

2. Improved Grid Testing and Validation: Addressing dynamics challenges and proposing enhanced control schemes for GEs can lead to the advancement of testing and validation methodologies for grid-connected systems. This benefits stakeholders such as grid operators and equipment manufacturers by enhancing the reliability and stability of grid-connected systems, ultimately improving grid performance.

3. Increasing Capacity of Renewable Energy into Power Grid: The refined control strategies proposed for challenges like transformer saturation and adverse interactions between GEs and Devices Under Test (DUTs) can enhance the reliability and stability of renewable energy integration into the power grid. This paves the way for increased capacity of renewable energy resources, fostering a healthier and more sustainable power grid infrastructure.

8. Appendices

Publications

[J1] Z. Li, X. Wang, F. Zhao, S. Munk-Nielsen, M. Geske, R. Grune, D. B. Rønnest Andersen and M. G. Rodriguez, "Power-hardware design and topologies of converter-based grid emulators for wind turbines," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 5, pp. 5001-5017, Oct. 2023, doi: 10.1109/JESTPE.2023.3302808.

[J2] Z. Li, F. Zhao, X. Wang, S. Munk-Nielsen, M. Geske, R. Grune, D. B. Rønnest Andersen and M. G. Rodriguez, "Medium-voltage megawatt power-electronic-based grid emulators: testing capability requirements and dynamics challenges – a review," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1545-1559, Apr. 2024, doi: 10.1109/JESTPE.2023.3268449.

[J3] Z. Li, F. Zhao, S. Munk-Nielsen, M. Geske and X. Wang, "Analysis and mitigation of transient overvoltage and voltage imbalance in submodule capacitors for MMC-based grid emulators," *IEEE J. Emerg. Sel. Topics Power Electron.*, Apr. 2024, early access, doi: 10.1109/JESTPE.2024.3387078.

[J4] Z. Li, F. Zhao, F. Hans, S. Munk-Nielsen and X. Wang, "Adaptive anti-saturation control design of transformers in converter-based grid emulators," *IEEE J. Emerg. Sel. Topics Power Electron.*, Apr. 2024, early access, doi: 10.1109/JESTPE.2024.3392449.

[C1] Z. Li *et al.*, "Testing requirements and control strategies of next-generation grid emulator: a review," in *Proc. Int. Power Electron. Conf. (IPEC-Himeji 2022- ECCE Asia),* Himeji, Japan, May 2022, pp. 1560-1566, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807056.

[C2] Z. Li, F. Zhao, X. Chen, S. Munk-Nielsen, M. Geske, R. Grune and X. Wang, "Analysis and mitigation of submodule capacitor overvoltage for MMC-based grid emulator under LVRT test," in *Proc. Wind. Solar Integration Workshop*, Hague, Netherlands, Oct. 2022, pp. 1-8, doi: 10.1049/icp.2022.2761.

[C3] X. Chen, Z. Li, F. Zhao, X. Wang, M. Geske and R. Grune, "Transformer saturation analysis and mitigation for MMC-based grid emulator," in *Proc. Int. Conf. Power Electron. (ICPE 2023 - ECCE Asia)*, Jeju Island, Korea, May 2023, pp. 2234-2238, doi: 10.23919/ICPE2023-ECCEAsia54778.2023.10213788.

[C4] Z. Li, F. Zhao, X. Chen, S. Munk-Nielsen and X. Wang, "Issues of impedance emulation of converter-based grid emulator for LVRT test," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Orlando, FL, USA, 2023, pp. 2741-2746, doi: 10.1109/APEC43580.2023.10131150.

[C5] Z. Li, F. Zhao, S. Munk-Nielsen and X. Wang, "Passivity-based co-design of active damping and voltage controller for converter-based grid emulator," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Orlando, FL, USA, 2023, pp. 1097-1101, doi: 10.1109/APEC43580.2023.10131405.

[T1] Z. Li, "Modeling and Control of Modular Multilevel Converter-Based Grid Emulators," PhD thesis, Aalborg University, Denmark, 2024.